z/OS Support for z13 Servers

Session 17444

Greg Daynes (@greg_daynes)
gdaynes@us.ibm.com
IBM STSM - z/OS Installation and Deployment Architect

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Agenda

- IBM z13 Overview
- z/OS Support by Release
- Hardware PSP Buckets and Fix Categories
- Migration Considerations
  - General
  - z13 Migration Considerations
  - Sysplex and Multisystem Considerations
  - Exploitation Considerations for Selected Functions
- Summary
- Backup

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IBM z13 System Functions and Features

Five hardware models
Up to 141 processors configurable as CPs, zIIPs, IFLs, ICFs or optional SAPs (no zAAPs) • 100-way on z/OS V1.12 or V1.13 • Up to 141-way on z/OS V2.1 (non-SMT mode) • Up to 128-way on z/OS V2.1 (SMT mode) - max active threads is 213
Up to 10 TB of Redundant Array of Independent Memory (RAIM) • 1 TB per z/OS LPAR on z/OS V1.12 or V1.13 • Up to 4 TB per z/OS LPAR on z/OS V2.1 (SoD)
Changed (node) cache structure
96 GB Fixed HSA
Improved Channel Subsystem Scalability • Up to 85 LPARs • Up to six logical channel subsystems (CSSs) • 4 Subchannel Sets per CSS
Single Instruction Multiple Data (SIMD) instruction set and execution
Two-way simultaneous multithreading (SMT) support for up to 128 cores (IFLs and zIIPs)
New and enhanced instructions
XL C/C++ ARCH(11) and TUNE(11) exploitation: • New z13 hardware instruction support • SIMD (Vector support) and Vector data • Decimal Floating Point packed conversion facility support • Performance improvements
IBM zAware: z/OS and Linux on System z

(z/OS support in blue)

CPU Measurement Facility
Flash Express (Storage Class Memory-SCM)
CF exploitation of Flash Express
IBM zEnterprise Data Compression (zEDC) capability using zEDC Express
OSA Express5S
Shared RoCE Express Support
Miscellaneous PCIe Enhancements • Greater than 256 PFID support • PCIe extended address translation • Enhanced the PCIe function definition • PCIe function measurement block changes
FICON Express16S
FICON Dynamic Routing
Improved zHPF I/O Execution at Distance
Fabric Priority for an I/O request
Support architecture for up to 85 Domains on Crypto Express5S
Crypto Express5S Exploitation • Next Generation Coprocessor support • Format Preserving Encryption (FPE)
Integrated Coupling Adapter (ICA) Links
Increases number of coupling CHPIDs from 128 to 256 per CEC
zBX Model 004 support

/Orlando-Eval

in Orlando 2015

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z/OS Support Summary

Release	z900/ z800 WdfM	z990/ z890 WdfM	z9 EC z9 BC WdfM	z10 EC z10 BC WdfM	z196 z114 WdfM	zEC12 zBC12	z13	End of Service	Extended Defect Support[1]
z/OS V1.12[1]	X	X	X	X	X	X	X	9/14[1]	9/17[1*]
z/OS V1.13	X	X	X	X	X	X	X	9/16*	9/19[1*]
z/OS V2.1			X	X	X	X	X	9/18*	9/21[1*]
z/OS 2.2*				X	X	X	X	9/20*	9/23[1*]

Notes:

1 Beginning with z/OS V1.12, IBM Software Support Services replaces the IBM Lifecycle Extension for z/OS offering with a service extension for extended defect support.

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

WdfM Server has been withdrawn from Marketing

Legend

Defect support provided with IBM Software Support Services for z/OS
Generally supported

Supported Releases

- **z13 capabilities differ depending on z/OS release**
  - Toleration support provided on z/OS V1.12
    - The IBM Software Support Services is required for extended defect support.
  - Exploitation support provided on z/OS V1.13 and higher
    - z/OS V1.13
      - Exploitation of selected functions
    - z/OS V2.1
      - Exploitation of most functions
    - z/OS V2.2*
      - Full exploitation planned in base

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

z/OS Toleration Support for z13

- z/OS V2.2*
- z/OS V1.13
- z/OS V1.12 (No longer generally supported as of September 30, 2014. IBM Software Support Services offers a service extension support for z/OS V1.12 for up to three years, beginning October 1, 2014 and available through September 30, 2017).

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

z/OS V1.12 Toleration Support for z13

- **Provides same functionality as that on the IBM zEC12 plus**
  - HiperDispatch
  - FICON Express8S
  - Parallel Sysplex InfiniBand (PSIFB) Coupling Links
  - CF Level 18 and 19 Support
  - Crypto Express4S toleration
  - Crypto Express4S Exploitation (if web deliverable is installed)
    - Enterprise Security PKCS11- Hardware Security Module (HSM), DUKPT for MAC and Data Encryption, Cipher Text Translate CCA Verb, PKDS/TKDS Constraint Relief, FIPS Evaluation, Common Criteria, Random Number Cache, FIPS on Demand, Wrapping Keys with Strong Keys
  - High Performance FICON for System z (zHPF)
  - OSA-Express5S (GbE LX and SX, 1000BASE-T, 10 GbE LR and SR)
  - GRS FICON CTC toleration
- **z/OS V1.12**
  - **FICON Express16S**
  - **Greater than 128 Coupling Links toleration**
  - **Crypto Express5S toleration**
    - **Treats Crypto Express5S as Crypto Express4S**
  - **Support architecture for up to 85 Domains on Crypto Express4S and Crypto Express5S**
  - **New z/Architecture Instructions (assembler new OPCODE support)**

z/OS Toleration Support for z13

- z/OS V2.2*
- z/OS V2.1
- **z/OS V1.13**
- z/OS V1.12 (No longer generally supported as of September 30, 2014. IBM Software Support Services offers a service extension support for z/OS V1.12 for up to three years, beginning October 1, 2014 and available through September 30, 2017).

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z/OS V1.13 Exploitation Support for z13

- **Provides same functionality as that on the IBM zEC12**
  - Java exploitation of the Transactional Execution Facility
  - Exploitation of New Hardware Features - C/C++ Arch(10)/Tune(10)
  - IBM zAware (z/OS Monitoring)
  - RSM Enhancements
    - Flash Express Support and 2 GB Large Page Support
  - CF Flash Support
  - CCA 4.4 and other cryptographic enhancement support:
    - RKX Key Export Wrap, UDX Reduction/Simplification, additional EP11 algorithms, expanded EMV support, AP Configuration simplification, CTRACE Enhancements, KDS Key Utilization Stats, DK AES PIN Phase 1, DK AES PIN support Phase 2, PKT UDX, PIN Migrate
- **All z13 functions available on z/OS V1.12 (prior slide) plus:**
  - **Changed (node) cache structure optimized by HiperDispatch**
  - **Greater than 128 Coupling Links per CEC**
  - **CF Level 20 support**
  - **Integrated Coupling Adapter (ICA) Links**
  - **Crypto Express5S exploitation (if web deliverable is installed)**
    - **Next Generation Coprocessor support, Format Preserving Encryption (FPE)**
  - **Improved Channel Subsystem Scalability**
    - **Up to 85 LPARs**
      - **Only up to 60 LPARs can be defined if z/OS V1.12 is running in one of the LPARs**
    - **Up to six logical channel subsystems (CSSs)**
    - **4 Subchannel Sets per CSS**
  - **Improved zHPF I/O Execution at Distance**
  - **Manage FICON Dynamic Routing**
  - **Fabric Priority for an I/O request**

z/OS Toleration Support for z13

- z/OS V2.2*
- **z/OS V2.1**
- z/OS V1.13
- z/OS V1.12 (No longer generally supported as of September 30, 2014. IBM Software Support Services offers a service extension support for z/OS V1.12 for up to three years, beginning October 1, 2014 and available through September 30, 2017).

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z/OS V2.1 Exploitation Support for z13

- **Provides same functionality as that on the IBM zEC12**
  - All functions available on z/OS V1.13 (prior slide) plus:
    - Support the transactional Execution Facility in additional production environments
    - IBM zEnterprise Data Compression (zEDC) capability using zEDC Express
    - Shared Memory Communications-Remote Direct Memory Access (SMC-R)
    - Support of PNETID for OSD and IQD CHPIDs and PCIe functions
- **All z13 functions available on z/OS V1.13 (prior slide) plus:**
  - **Shared RoCE Support**
  - **Two-way simultaneous multithreaded (SMT) operation for IFLs and zIIPs**
  - **Up to 141-way in non-SMT mode (up to 128 way in SMT mode)**
  - **Increase number of coupling links from 128 to 256 per CEC**
  - **Health Check for FICON Dynamic Routing**
  - **Miscellaneous PCIe enhancements**
    - PCIe extended address translation
    - Greater than 256 PFID support
    - Add PCIe function type to the PCIe function definition in the I/O configuration
    - PCIe function measurement block changes
  - **Single Instruction Multiple Data (SIMD) instruction set and execution**
    - MASS and ATLAS Library, SPSS Modeler and ILOG Cplex
  - **Exploitation of new hardware instructions – XL C/C++ ARCH(11) and TUNE(11)**
    - New z13 hardware instruction support
    - SIMD (Vector support) and Vector data
    - Decimal Floating Point packed conversion facility support
    - Performance improvements
  - **Up to 4 TB per z/OS LPAR (statement of direction)**

Supported z/OS Releases and ICSF Levels

- **z/OS V1.12 Crypto customers can run with:**
  - **HCR7770 – Base z/OS V1.12[1]**
  - **HCR7780 – Cryptographic Support for z/OS V1R10-V1R12**
  - **HCR7790 – Cryptographic Support for z/OS V1R11-V1R13**
  - **HCR77A0 – Cryptographic Support for z/OS V1R12-V1R13**
- **z/OS V1.13 Crypto customers can run with:**
  - **HCR7780 – Base z/OS V1.13**
  - **HCR7790 – Cryptographic Support for z/OS V1R11-V1R13**
  - **HCR77A0 – Cryptographic Support for z/OS V1R12-V1R13**
  - **HCR77A1 – Cryptographic Support for z/OS V1R13-z/OS V2R1**
  - **HCR77B0 – Enhanced Cryptographic Support for z/OS V1R13-z/OS V2R1**
- **z/OS V2.1 Crypto customers can run with:**
  - **HCR77A0 – Base z/OS V2.1**
  - **HCR77A1 – Cryptographic Support for z/OS V1R13-z/OS V2R1**
  - **HCR77B0 – Enhanced Cryptographic Support for z/OS V1R13-z/OS V2R1**
- **z/OS V2.2* Crypto customers can run with:**
  - **HCR77B0 – Planned to be part of the base in z/OS V2.2**

1 – not supported on a z13

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z/OS Support Summary

Release	IBM.Device.Server.z13-2964.RequiredService										IBM.Device.Server.z13-2964.Exploitation																							
	Base Support	CPU Measurement Facility	Crypto Express5S Toleration	FICON Express 8S	FICON Express 16S	z13 Assembler Support	OSA-Express4S	OSA-Express5S	GRS Support for FICON CTCs	High Performance FICON (zHPF)	InfiniBand Coupling Links	Support for 256 Coupling Links/CEC	>16 Cryptographic Domains	CF Level 20 Support	Integrated Coupling Links (ICA SR)	SAN Fabric I/O Priority	FICON Dynamic Routing	Improved CSS Scalability	zAware	Transactional Memory	Improved zHPF I/O Execution at Distance	zEnterprise Data Compression (zEDC)	Flash Express	2GB Large Pages	Crypto Express5S Exploitation	Shared ROCE Express Support	Simultaneous Multithreading (SMT)	Miscellaneous PCIe Enhancements	Greater than 100 CPs per z/OS Image[3]	Single Instruction Multiple Data (SIMD)	z13 XL C/C++ Support	Up to 4TB per z/OS LPAR
z/OS V1.12[1]	Y	Y	W	Y	Y	Y	Y	Y	Y	Y	Y	T	W									T										
z/OS V1.13	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	T	W	W	W							
z/OS V2.1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	W	Y	Y	Y	Y	Y	W	Y[4]
z/OS 2.2[2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Notes:

1 Beginning with z/OS V1.12, IBM Software Support Services replaces the IBM Lifecycle Extension for z/OS offering with a service extension for extended defect support.

2 Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

3 Up to 141-way in non-SMT mode (up to 128-way in SMT mode)

4 Up to 4TB per z/OS is a statement of direction for z/OS V2.1

T Coexistence support provided

W A web deliverable is required for exploitation support available at http://www-03.ibm.com/systems/z/os/zos/downloads/

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z13 PSP Bucket and Fix Categories

- Support provided via a combination of web deliverables and PTFs
  - Documented in PSP Bucket: **Upgrade = 2964DEVICE, Subset = 2964/ZOS**
  - Unlike prior server generations PSP buckets, actual PTFs are not listed in the PSP bucket, just pointers to SMP/E Fix Categories, and any web deliverables needed for exploitation
  - As in the past, if you are skipping generations of servers, you need to install all the maintenance and perform required migration actions for the servers that you are skipping:

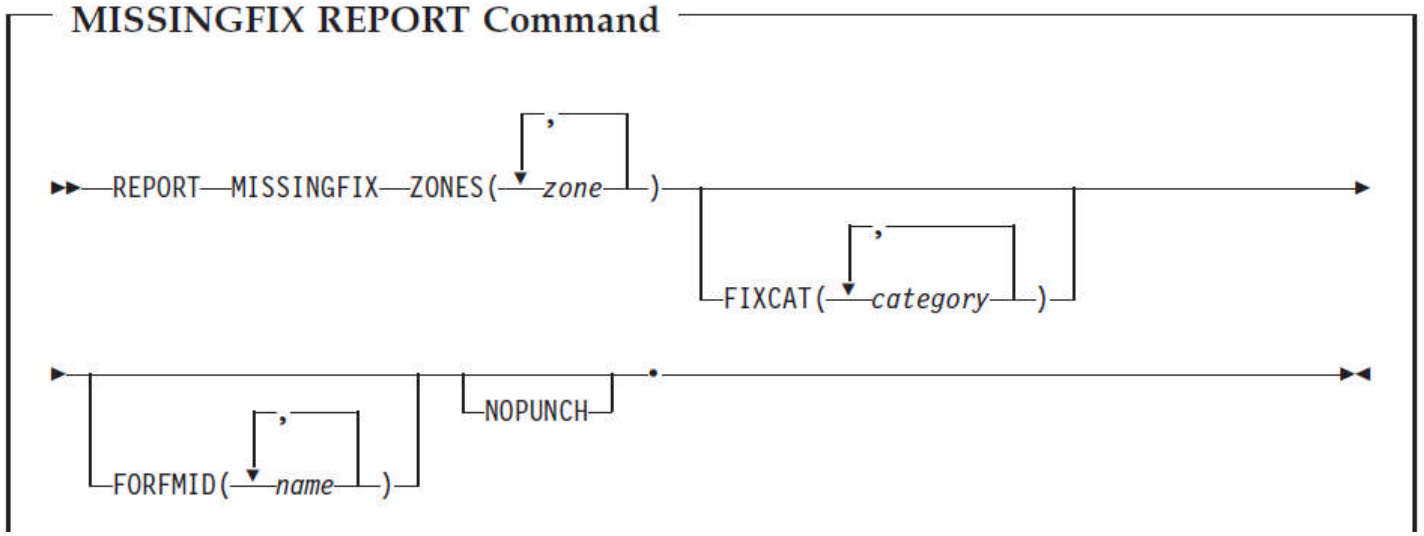
Server	UPGRADE	Subset	Fix Category
zBC12	2828DEVICE	2828/ZOS	IBM.Device.Server.zBC12-2828*
zEC12	2827DEVICE	2827/ZOS	IBM.Device.Server.zEC12-2827*
z114	2818DEVICE	2818/ZOS	IBM.Device.Server.z114-2818*
z196	2817DEVICE	2817/ZOS	IBM.Device.Server.z196-2817*
z10 BC	2098DEVICE	2098/ZOS	IBM.Device.Server.z10-BC-2098*
z10 EC	2097DEVICE	2097/ZOS	IBM.Device.Server.z10-EC-2097*
z9 BC	2096DEVICE	2096/ZOS	IBM.Device.Server.z9-BC-2096*
z9 EC	2094DEVICE	2094/ZOS	IBM.Device.Server.z9-EC-2094*
z890	2086DEVICE	2086/ZOS	IBM.Device.Server.z890--2086*
z990	2084DEVICE	2084/ZOS	IBM.Device.Server.z990-2084*

Other Fix Categories of Interest

- **Other PTFs related to z13 (common to other servers) can be identified by the following Fix Categories:**
  - **IBM.Device.Server.*.ParallelSysplexInfiniBandCoupling**
  - **IBM.Device.Server.*.ServerTimeProtocol**
  - **IBM.Device.Server.*.zHighPerformanceFICON**
  - **IBM.Device.Server.*.UnifiedResourceManager**
  - **IBM.Function.zEDC**
  - **DB2.AnalyticsAccelerator***
- **PTFs that allow prior levels of ICSF to coexist with, and fallback from, the Enhanced Cryptographic Support for z/OS V1.13 and z/OS V2.1 web deliverable**
  - **IBM.Coexistence.ICSF.z/OS_V1R13-V2R1-HCR77B0**

REPORT MISSINGFIX Command Syntax

Sample Command:



Operands:

- **ZONES** - identifies one or more target and distribution zones to report on
- **FIXCAT** –
  - Identifies Fix Categories of interest (aka Interest List)
  - Determines which FIXCAT HOLDs will be included in the report
  - Extended wildcards * and % can be used to express generic interests
- **FORFMID** - limits which FIXCAT HOLDs will be included in the report
- **NOPUNCH** - indicates that SMP/E should not write any output to SMPPUNCH

SMP/E Report MISSINGFIX …

Sample Command to identify missing fixes for:

- z/OS V1.12, z/OS V1.13 and z/OS V2.1
- Required, Exploitation and Recommended service for a z13
- All service for a zEC12
  - Either because skipping that generation or it has been a while since zEC12 maintenance was checked/installed
- All hardware related, but not z13 specific, categories

```
SET BDY(GLOBAL) .
REPORT MISSINGFIX ZONES(TGT112,TGT113,TGT21)
          FIXCAT(IBM.Device.Server.z13-2964.RequiredService,
                 IBM.Device.Server.z13-2964.Exploitation,
                 IBM.Device.Server.z13-2964.RecommendedService,
                 IBM.Device.Server.zEC12*,
                 IBM.Device.Server.zBC12*,
                 IBM.Device.Server.*.ParallelSysplexInfiniBandCoupling,
                 IBM.Device.Server.*.ServerTimeProtocol,
                 IBM.Device.Server.*.zHighPerformanceFICON,
                 IBM.Device.Server.*.UnifiedResourceManager,
                 IBM.Function.zEDC,
                 IBM.DB2.AnalyticsAccelerator*) .
```

SMP/E Report MISSINGFIX …

- **Snippet of a REPORT MISSINGFIX output for a z/OS V2.1 system**

```
MISSING FIXCAT SYSMOD REPORT FOR ZONE TGT21

                          HOLD      MISSING   HELD      _____RESOLVING SYSMOD_____
FIX CATEGORY      FMID    CLASS     APAR      SYSMOD    NAME      STATUS  RECEIVED
________________  _______ ________  ________  ________  ________  ______  _________
IBM.Device.Server.z13-2964.RequiredService
                  EER3500           AO20501   EER3500   UO01758   GOOD    NO
                  HBB7790           AA46642   HBB7790   UA75881   GOOD    NO
                  HCR77A0           AA45547   HCR77A0   UA76041   GOOD    NO
                  HCR77A1           AA45547   HCR77A1   UA76042   GOOD    NO
                  HCS7790           AA44294   HCS7790   UA75914   GOOD    NO
                  HIO1104           AA44637   HIO1104   UA90773   GOOD    NO
                  HMQ4160           AI22786   HMQ4160   UI24510   GOOD    NO
                                    AM79901   HMQ4160   UI24397   GOOD    NO
                  HSAL110           AA46903   HSAL110   UA76072   GOOD    NO
                  HWRE330           AA45346   HWRE330   UA75591   GOOD    NO
                  HWRE340           AA45346   HWRE340   UA75592   GOOD    NO
                  HWRE350           AA46560   HWRE350   UA75887   GOOD    NO
                  JCS779J           AA44294   JCS779J   UA75915   GOOD    NO
                  JWRE331           AA46560   JWRE331   UA75876   GOOD    NO
                  JWRE341           AA46560   JWRE341   UA75890   GOOD    NO
                  JWRE351           AA46560   JWRE351   UA75891   GOOD    NO
```

z/OS Support for z13

- **Base support is provided by PTFs identified by:**
  - **IBM.Device.Server.z13-2964.RequiredService**
- **Exploitation of many functions is provided by PTFs identified by:**
  - **IBM.Device.Server.z13-2964.Exploitation**
- **Recommended service is identified by:**
  - **IBM.Device.Server.z13-2964.RecommendedService**
    - Should also be either “required service” or “exploitation”
- **Exploitation of some functions requires a web deliverable**
  - Exploitation of Crypto Express5S requires the ***Enhanced Cryptographic Support for z/OS V1.13 and z/OS V2.1*** web deliverable
  - Exploitation of new hardware instructions using XL C/C++ ARCH(11) and TUNE(11) or SIMD exploitation by MASS and ATLAS Libraries, requires the ***XL C/C++ V2R1M1 web deliverable with z13 support for z/OS 2.1*** web deliverable
  - Exploitation of Flash Express or 2GB Large pages on z/OS V1.13 requires the **z/OS V1.13 RSM Enablement** web deliverable
- **All support is planned to be included in the z/OS V2.2* base**

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General Migration Considerations

- **z/OS releases do not require z13 servers**
- **z13 servers ONLY require software identified as 'base' support**
  - Minimal toleration support needed depending on z/OS release
  - z13 servers do NOT require any 'functional' software
    - However, I recommend installing all z13 service prior to upgrading your hardware
- **z13 capabilities differ depending on z/OS release**
  - Web deliverables are needed for some functions on some releases
- **Don't migrate software releases and hardware at the same time**
- **Keep members of the sysplex at the same software level other than during brief migration periods**
- **Review any restrictions and migration considerations prior to creating upgrade plan**

General Recommendations and Considerations

- **z13 servers are based on existing System z technology**
  - z/Architecture (z900/z800)
  - Multiple Logical Channel Subsystems (z990/z890)
  - OSA-Express2, FICON Express4, Crypto Express2 (z9 EC/z9 BC)
  - HiperDispatch, Large Page, zHPF (z10 EC, z10 BC)
  - Ensembles, native PCIe-based I/O – FICON Express8S and OSA Express4S (z196, z114)
  - Flash Express, RoCE, and zEDC (zEC12/zBC12)
- **Very few new migration issues identified**
  - z990, z890, z9 EC, z9 BC, z10 EC, z10 BC, z196, z114, zEC12, and zBC12 server migration actions “inherited”
  - Many functions are enabled/disabled based on the presence or absence of the required hardware and software.
    - Some functions have exploitation or migration considerations (subsequent charts)

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Unsupported Hardware Features

- **The following hardware features cannot be ordered and cannot be carried forward from an upgrade on an earlier server to the z13 server.**
  - **HCA2-O**
  - **HCA2-O LR**
  - **ISC-3 links**
  - **CHPID type OSN (OSA-Express for NCP) is not supported on OSA-Express5S GbE LX**
  - **Crypto Express3**
  - **Crypto Express4S**
  - **STP Mixed CTN**
    - The zEC12 and zBC12 were the last z Systems servers to support connections to an STP Mixed CTN. This also includes the Sysplex Timer (9037).
    - Starting with z13, servers that require Time synchronization, such as to support a base or Parallel Sysplex, will require Server Time Protocol (STP) and all servers in that network must be configured in STP-only mode.
  - **IBM System z Application Assist Processor (zAAP)**
    - IBM continues to support running zAAP workloads on IBM System z Integrated Information Processors (zIIPs).
      - IBM has removed the restriction preventing zAAP-eligible workloads from running on zIIPs when a zAAP is installed on the CEC.
      - This was intended to help facilitate migration and testing of zAAP workloads on zIIPs. With a z13, one CP must be installed with the installation of any zIIPs or prior to the installation of any zIIPs.
      - The total number of zIIPs purchased cannot exceed twice the number of CPs purchased. However, for upgrades from zEC12s with zAAPs, conversions from zAAPs may increase this ratio to 4:1.

New z/Architecture Machine Instructions

- **OPTABLE option now supports ZS7**
  - The assembler loads and uses the operation code table that contains the symbolic operation codes for the machine instructions specific to z/Architecture systems with the general instructions extensions facility and z13 instructions.
- **The new mnemonics may collide with (be identical to) the names of Assembler macro instructions you use**
  - If you write programs in Assembler Language, you should compare the list of new instructions to the names of Assembler macro instructions you use and/or provide
  - If a conflict is identified, take one of these actions:
    - Change the name of your macro instruction.
    - Specify a separate assembler OPCODE table
      - via PARM= , ASMAOPT, or '*PROCESS OPTABLE….' in source
    - Use a coding technique that permits both use of a new instruction and a macro with the same name in an assembly such as HLASM's Mnemonic tags (:MAC :ASM)
- **For a job to assist in identifying assembler macro instructions which conflict with z13 hardware instructions see PRS5289 on Techdocs:**
  - *http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/PRS5289*

Crypto Express5S and TKE (Trusted Key Entry)

- **On a z13, TKE 8.0 can be used to manage the new Crypto Express5S cards.**
- **If a TKE is used, the ICSF level needs to be:**
  - HCR77B0 (or higher) or
  - HCR77A0/HCR77A1 in toleration mode with the PTFs for APARs OA45547 and OA44910
- **The configuration migration tasks feature of the TKE was enhanced to also support the Crypto Express5S coprocessor.**
  - You can use TKE 8.0 to collect data from previous generations of Cryptographic modules and apply the data to Crypto Express5S coprocessors.

HCD Activation Support

- **Dynamic activation is supported on z/OS V2.1 and z/OS V2.2**
- **Dynamic activation is restricted on z/OS V1.13 and below:**
  - **z/OS V1.13** allows no hardware activation, if PCIe functions or the PNETID attribute for channel paths is defined.
    - There is only limited software activation with hardware validation support.
  - **z/OS V1.12**
    - Has the same restrictions as z/OS V1.13 but further does not allow hardware activation if any of the following are defined:
      - The CS5 CHPIDs
      - More than 128 coupling CHPIDs defined for the CEC,
      - There are devices in subchannel set 3.
    - There is only limited software validation with hardware validation support.
      - Changes to the CS5 CHPIDs are ignored for software activation.
- **IBM recommends that you define and activate all the new hardware definitions on a z/OS V2.1 (or higher) system with the appropriate HCD/HCM PTFs installed and only perform software activates (with hardware validation) on lower level systems.**

HCD Compatibility

Release	Funct	z900/ z800 WdfM	z990/ z890 WdfM	z9 EC z9 BC WdfM	z10 EC z10 BC WdfM	z196 Z114 WdfM	zEC12 zBC12 w/o PCIE	zEC12 GA2 zBC12 w/PCIE	z13 w/o PCIE	z13 w/PCIE
z/OS V1.12	HW	Y	Y	Y	Y	Y	Y	N	N	N
	SW	Y	Y	Y	Y	Y	Y	Y	Y[1]	Y[1]
	UPD	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RPT	Y	Y	Y	Y	Y	Y	Y	Y	Y
z/OS V1.13	HW	Y	Y	Y	Y	Y	Y	N	Y	N
	SW	Y	Y	Y	Y	Y	Y	Y	Y	Y
	UPD	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RPT	Y	Y	Y	Y	Y	Y	Y	Y	Y
z/OS V2.1	HW			Y	Y	Y	Y	Y	Y	Y
	SW			Y	Y	Y	Y	Y	Y	Y
	UPD			Y	Y	Y	Y	Y	Y	Y
	RPT			Y	Y	Y	Y	Y	Y	Y
z/OS V2.2	HW				Y	Y	Y	Y	Y	Y
	SW				Y	Y	Y	Y	Y	Y
	UPD				Y	Y	Y	Y	Y	Y
	RPT				Y	Y	Y	Y	Y	Y

HW – Perform hardware activate of selected processor
SW – Perform software activation, if IODF contains selected processor
UPD - Update selected processor (attributes) via HCD dialog
RPT - run reports on selected processors (attributes)

w/o PCIe – no PCIe functions are defined in the IODF and that no PNETIDs are used
1 - Changes to the CS5 CHPIDs are ignored for software activation.

CPU Measurement Facility

- **The number of CPU measurement facility counters for z13 remains at 128.**
- **While the structure of the SMF 113 Record does not change**, the values, interpretations, and frequency of certain sections do change; therefore, current tools using the data need to be updated for z13. For example, consider the following SMF record field:
  - **SMF113_2_CtrVN2** identifies how to interpret the MT-Diagnostic, Crypto and Extended counter sets.
    - As described in The IBM CPU Measurement Facility Extended Counters Definition for z10 and z196, SA23-2260, this field is set to 1 (for z10), 2 (for z196 or z114), or 3 (for zEC12 and zBC12), 4 (for z13).
  - **Note: As of z/OS V2.1, if you use the CPU Measurement Facility, IBM recommends:**
    - **Customers collect SMF 113 subtype 1 and 2 records**

Use of LOADxx MACHMIG Statements

- **MACHMIG**
  - Identifies one or more facilities that you do not want z/OS to use at this time because migration to another processor, z/OS release, or both is underway.
  - Code the MACHMIG statement as follows:
    - Column Contents
      - 1-7 MACHMIG
      - 10-72 A list of facilities not to use. When more than one facility is listed, separate each from the previous by one or more blanks or commas. The following facilities may be specified in upper, lower, or mixed case:
        - » EDAT2 - the hardware-based enhanced-DAT facility 2
        - » TX - the hardware-based transactional-execution facility
        - » VEF – the hardware-based vector registers (VR) in support of SIMD
  - A maximum of 3 MACHMIG statements are allowed
  - Default: None.
    - If you do not specify a MACHMIG statement, the system does not limit its use of machine facilities.

Use of LOADxx MACHMIG Statements …

- **Example**
  - The following example shows a MACHMIG statement that tells the system not to use the enhanced DAT facility 2, the transactional execution facility, and SIMD.

```
----+----1----+----2----+----3----+
MACHMIG   EDAT2,TX,VEF
```

- **Operand on DISPLAY IPLINFO**
  - DISPLAY IPLINFO LOADXX,MACHMIG command
    - Displays all the relevant MACHMIG statements from the LOADxx PARMLIB member, or indicates that there were none.

Agenda

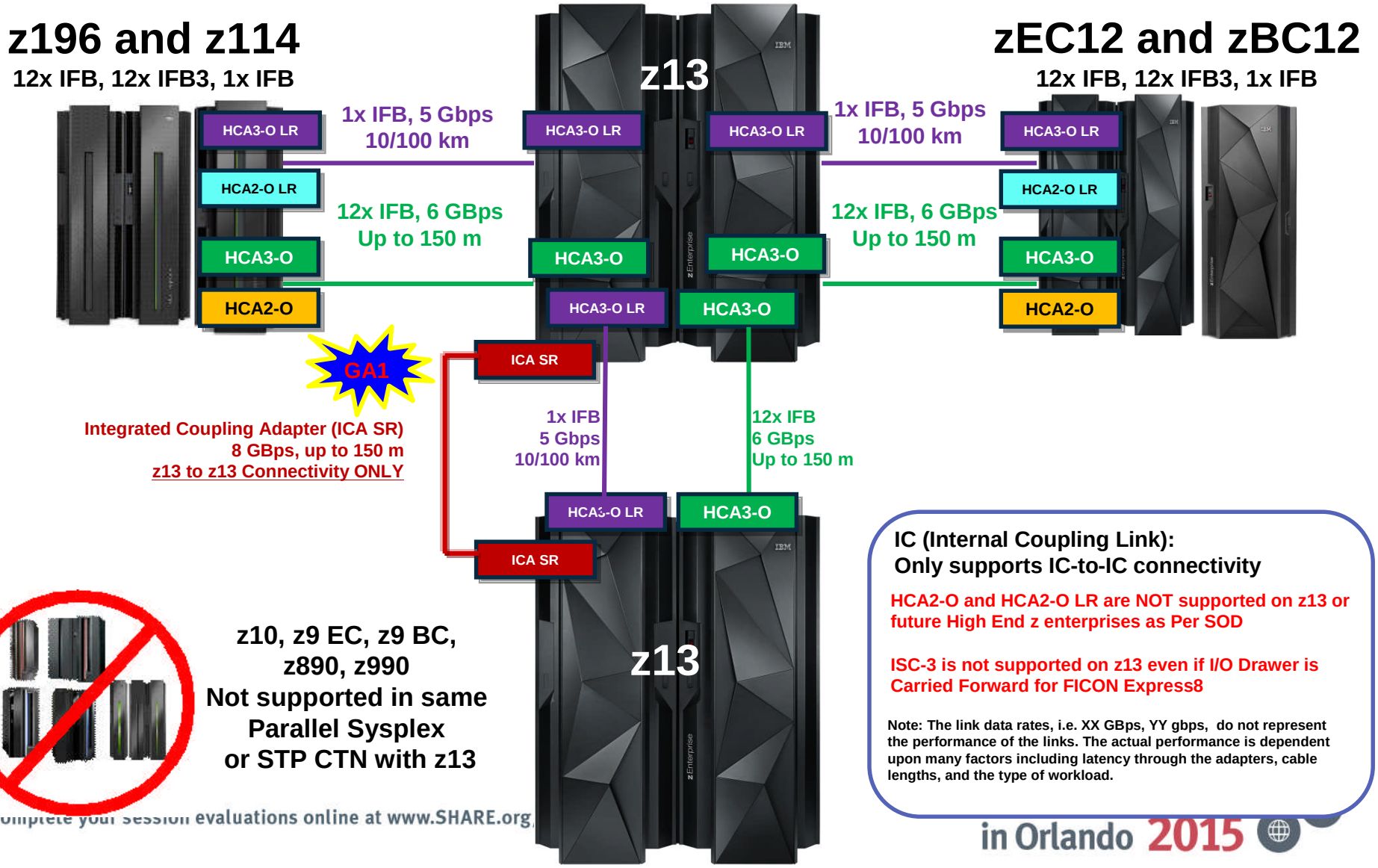
- IBM z13 Overview
- z/OS Support by Release
- Hardware PSP Buckets and Fix Categories
- **Migration Considerations**
  - General
  - z13 Migration Considerations
  - **Sysplex and Multisystem Considerations**
  - Exploitation Considerations for Selected Functions
- Summary
- Backup

Server Participation in a Parallel Sysplex

- **z13 servers do not support active participation in the same Parallel Sysplex with:**
  - IBM System z10 Enterprise Class (z10 EC), IBM System z10 Business Class (z10 BC)
  - IBM System z9 Enterprise Class (z9 EC), IBM System z9 Business Class (z9 BC)
  - IBM eServer zSeries 990 (z990), IBM eServer zSeries 890 (z890)
  - IBM eServer zSeries 900 (z900), IBM eServer zSeries 800 (z800)
  - Older System/390 Parallel Enterprise Server systems

  This means:
  - Configurations with z/OS on one of these servers can't add a z13 server to their sysplex for either a z/OS image or a CF image
  - Configurations with a CF on one of these servers can't add a z13 server to their sysplex for either a z/OS image or a CF image

z13 Parallel Sysplex Coupling Connectivity



z10, z9 EC, z9 BC, z890, z990 Not supported in same Parallel Sysplex or STP CTN with z13

IC (Internal Coupling Link):
Only supports IC-to-IC connectivity

HCA2-O and HCA2-O LR are NOT supported on z13 or future High End z enterprises as Per SOD

ISC-3 is not supported on z13 even if I/O Drawer is Carried Forward for FICON Express8

Note: The link data rates, i.e. XX GBps, YY gbps, do not represent the performance of the links. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.

z13 Parallel Sysplex Coupling Connectivity

- **zEC12/zBC12 were the last generation to support ISC-3, (12X) HCA2-O, (1X) HCA2-O LR, and participate in a Mixed CTN**
  - For z13, you must migrate to ICA or Coupling over Infiniband; and STP only CTNs
- **ISC-3 Migration:**
  - Evaluate your current ISC-3 usage (long distance, short distance, coupling data, timing only, etc.) to determine how to fulfill ISC-3 requirements with the links available on z13
  - Clients can migrate from ISC-3 to ICA, 12X, or 1X on z13

Integrated Coupling Adapter (ICA) Links

- **IBM Integrated Coupling Adapter (ICA SR)**
  - PCIe is the overwhelming industry standard interface for high-speed, differential communication
  - z13 begins transition to PCIe for Coupling Connectivity with a new link type (CHPID type CS5)
  - ICA SR is recommended for short distance coupling z13 to z13
  - No performance degradation compared to coupling over Infiniband 12X IFB3 protocol on z13
- **Coupling over Infiniband (12X HCA3-O, 1X HCA3-O LR)**
  - Coupling over Infiniband is required for coupling z13 back to N-1 and N-2 generations
    - N-1: z13 to zEC12 / zBC12
    - N-2: z13 to z196 / z114
  - 12X HCA3-O short distance; 1X HCA3-O LR long distance
  - 1X HCA3-O LR is required for z13 to z13 long distance coupling

STP Configurations

- **Two types of Coordinated Timing Network (CTN) configurations were possible:**
  - **Mixed CTN**
    - Allows servers/CFs that can only be synchronized to a Sysplex Timer (ETR network) to coexist with servers/CFs that can be synchronized with CST in the “same” timing network
    - Sysplex Timer provides timekeeping information
    - zEC12 and zBC12 are the last System z servers to support connections to an STP Mixed CTN
    - **z13 does NOT support connections to a Mixed CTN**
  - **STP-only CTN**
    - All servers/CFs synchronized with CST
    - Sysplex Timer is NOT required
    - **z13 must participate in an STP-only CTN**

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Exploitation Considerations for Selected Functions

- CF Level 20
- Integrated Coupling Adapter (ICA) Links
- Increase number of coupling links from 128 to 256 per CEC (STP)
- Improved Channel Subsystem Scalability
  - 4 Subchannel Sets per CSS
- Fabric Priority for an I/O request
- Improved zHPF I/O Execution at Distance
- Manage FICON Dynamic Routing
- Health Check for FICON Dynamic Routing
- Crypto Express5S exploitation (if web deliverable is installed)
  - Next Generation Coprocessor support and Format Preserving Encryption (FPE)
- Two-way simultaneous multithreaded (SMT-2) operation
- Miscellaneous PCIe enhancements
- Shared RoCE Support
- XL C/C++ exploitation of new hardware instructions - ARCH(11) and TUNE(11)
- Single Instruction Multiple Data (SIMD) instruction set and execution

CF Level 20 Exploitation

- **Coupling Facility Use of Large Memory**
  - Designed to improve availability for larger CF cache structures and data sharing performance with larger DB2 Group Buffer Pools (GBP).
  - This support removes inhibitors to using large CF cache structures, enabling use of Large Memory to appropriately scale to larger DB2 Local Buffer Pools (LBP) and Group Buffer Pools (GBP) in data sharing environments.
  - To learn more about the performance benefits of large DB2 structures, reference *IBM zEnterprise System: Performance Report on Exploiting Large Memory for DB2 Buffer Pools with SAP* at http://www.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/WP102461
- **Structure and CF Storage Sizing with CFCC level 20**
  - May increase storage requirements when moving from:
    - CF Level 19 (or below) to CF Level 20
    - CF Sizer Tool recommended
      - http://www.**ibm.com**/systems/z/cfsizer/
      - Available since February 27, 2015
  - Similar to prior levels, ensure that the CF LPAR has at least 512MB of storage

Integrated Coupling Adapter (ICA) Links Exploitation Considerations

- **PCIe I/O for Future Coupling Connectivity**
  - Recognize the new CHPID type and allow XES to register as the owner off the CHPID type. This allows the CHPID type to be displayed in the D M=CHP command and to be configured online and offline.
  - Recognize the new CHPID type as a coupling related CHPID type and route control to XES to handle CHPID related events.
  - Allow an ACTIVATE command to be performed to dynamically add CS5 CHPIDs to the I/O configuration.
  - To provide extended path attributes when the enhanced-reporting-of-channel-path-characteristics (ERCPC) facility is active (the XES IXLYAMDA interface).
  - Ensure timing link related messaging is issued based on the configuration of the physical (not virtual) resources.
  - RMF data gatherers store information into Monitor III table CFIG3 and SMF record 74.4.
  - Minor changes to the corresponding report sections of the RMF Postprocessor CF Activity report (Subchannel Activity section and CF to CF Activity section) as well as to the Monitor III CFSYS Report

Note: RMF reports must be taken on highest release in Parallel Sysplex

RMF Coupling Facility Activity Report for ICA Links

C O U P L I N G F A C I L I T Y A C T I V I T Y

PAGE 7

z/OS V2R1 SYSPLEX UTCPLXW4 DATE 05/16/2011 INTERVAL 002.00.000
RPT VERSION V2R1 RMF TIME 02.28.00 CYCLE 01.000 SECONDS

COUPLING FACILITY NAME = X7CFR89

SUBCHANNEL ACTIVITY

SYSTEM NAME	# REQ TOTAL AVG/SEC	-- CF LINKS -- TYPE	GEN	USE	PTH BUSY	REQUESTS	# REQ	-SERVICE TIME(MIC) AVG	STD_DEV	DELAYED REQUESTS	# REQ	% OF REQ	AVG TIME(MIC) /DEL	STD_DEV	/ALL
R72	770185	CFP	2	2	0	SYNC	449208	20.1	[illegible]	LIST/CACHE	0	0.0	0.0	0.0	0.0
	855.8	CIB	3	3		ASYNC	238314	100.[illegible]	51[illegible]	LOCK	0	0.0	0.0	0.0	0.0
	401	CS5	1	1		ASYNC	38314	[illegible].9	49,[illegible]	LOCK	0	0.0	0.0	0.0	0.0
		SUBCH	142	142		CHANGED	0	[illegible]ED IN SYNC		TOTAL	0	0.0			
						UNSUCC		0	0.0						
R73	670185	CFP	2	2	0	SYNC	[illegible]8	0.1	15.8	LIST/CACHE	0	0.0	0.0	0.0	0.0
	655.8	SUBCH	12	12		ASYNC	238[illegible]	[illegible].9	51.2	LOCK	0	0.0	0.0	0.0	0.0
						CHANGED		INCLUDED IN ASYNC		TOTAL	0	0.0			
						[illegible]	0	0.0	0.0						

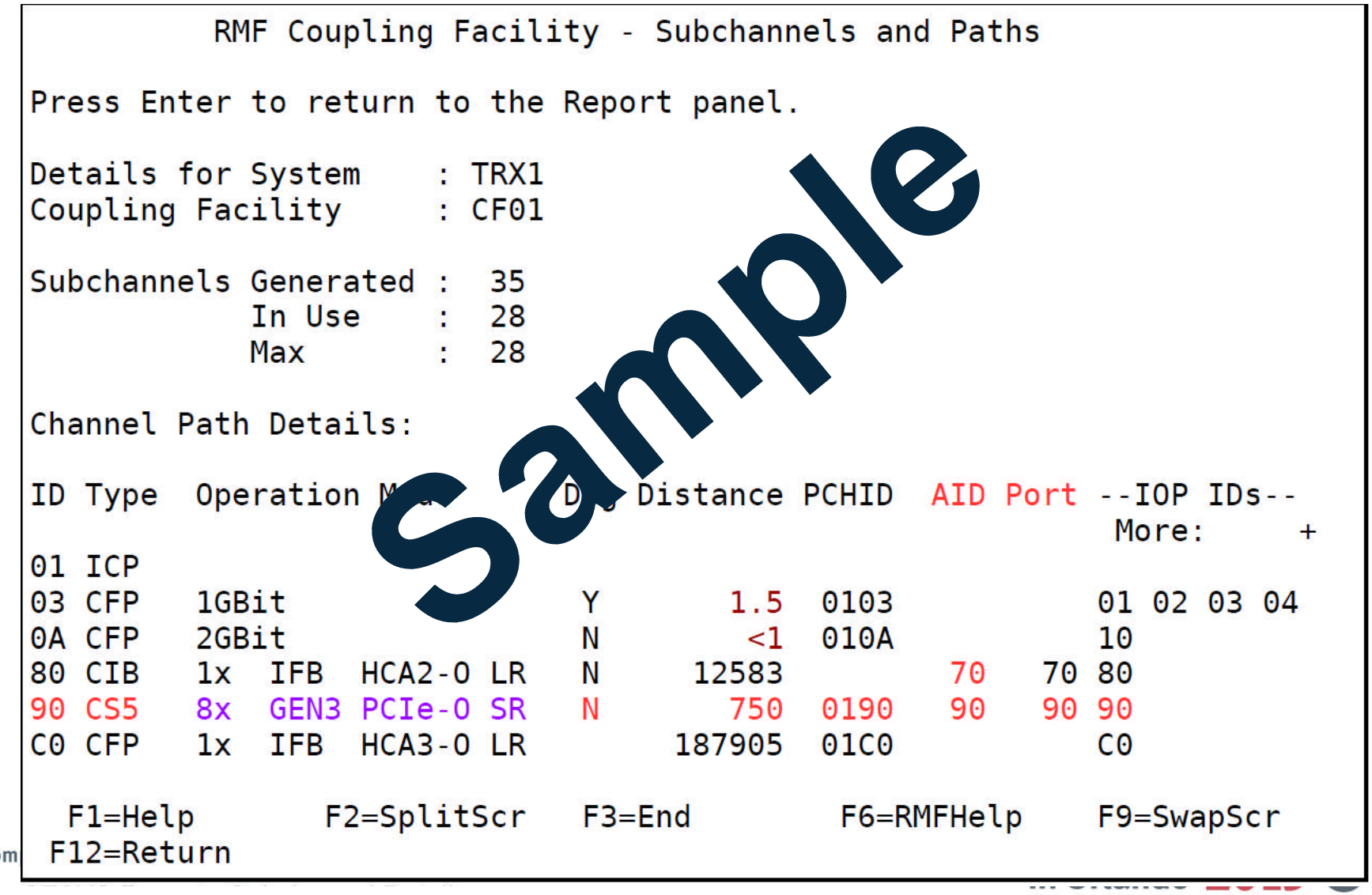
CHANNEL PATH DETAILS

SYSTEM NAME	ID	TYPE	OPERATION MODE	DEGRADED	DISTANCE	PCHID	AID	PORT	IOP IDS			
R72	01	CIB	1X IFB HCA2-O LR	Y	125		00	00	01	03	06	08
	02	CIB	12X IFB HCA3-O	N	1.5		10	01	06	06		
	03	CIB	1X IFB HCA2-O LR	Y	<1		00	01	01			
	04	CS5	8x GEN3 PCIe-O SR	N	19.9	104	10	02	06			
	A0	CFP	1GBIT	N	12345	1A0			0A	12		
	A1	CFP	2GBIT		33335	1A1			0A			
R73	B0	CFP	2GBIT	N	2125	1B0			02			
	B1	CFP	1GBIT	Y	325	1B1			02			

RMF Coupling Facility Activity Report for ICA Links

```
                              C O U P L I N G   F A C I L I T Y   A C T I V I T Y
                                                                                              PAGE  26
   z/OS V2R1            SYSPLEX UTCPLXW4          START 05/16/2011-04.00.00    INTERVAL 001.22.00
                        RPT VERSION V2R1 RMF      END   05/16/2011-05   00    CYCLE 01.000 SECONDS

------------------------------------------------------------------------------------------------------
 COUPLING FACILITY NAME = CFFR35B
------------------------------------------------------------------------------------------------------
                                          CF TO CF ACTIVITY
------------------------------------------------------------------------------------------------------
           # REQ                                 ----------- REQUESTS -----------    --------------- DELAYED REQUESTS ---------------
 PEER      TOTAL        -- CF LINKS --                  #   -SERV TIME(MIC)-                #    % OF   ------ AVG TIME(MIC) ------
 CF        AVG/SEC      TYPE        USE               REQ     AVG    STD_DEV              REQ    REQ     /DEL     STD_DEV     /ALL

 FR52CF3  413359        CIB           1      SYNC   41  9     0.0      0.0      SYNC     0     0.0     0.0        0.0       0.0
           114.8        CFP           1
 FR52CF4    1098        CS5           1      SYNC   10         .0      0.0      SYNC     0     0.0     0.0        0.0       0.0
             0.3        ICP           1

------------------------------------------------------------------------------------------------------
                                          CHANNEL PATH DETAILS
------------------------------------------------------------------------------------------------------
 PEER CF   ID   TYPE   OPERATION MODE      DEGRADED   DISTANCE

 FR52CF3   01   CIB    1X  IFB  HCA2-O LR                  125
           A0   CFP    1GBIT                  Y              0
 FR52CF4   51   CS5    8x  GEN3 PCIe-O SR     N            1.1
           21   ICP
```

RMF Coupling Facility Activity Report for ICA Links



```
          RMF Coupling Facility - Subchannels and Paths

Press Enter to return to the Report panel.

Details for System    : TRX1
Coupling Facility     : CF01

Subchannels Generated :  35
            In Use    :  28
            Max       :  28

Channel Path Details:

ID Type  Operation Mode                 D  Distance PCHID  AID Port --IOP IDs--
                                                                More:     +
01 ICP
03 CFP   1GBit                         Y       1.5  0103           01 02 03 04
0A CFP   2GBit                         N        <1  010A           10
80 CIB   1x  IFB  HCA2-O LR            N     12583                70   70 80
90 CS5   8x  GEN3 PCIe-O SR            N       750  0190   90      90 90
C0 CFP   1x  IFB  HCA3-O LR                 187905  01C0           C0

  F1=Help       F2=SplitScr   F3=End        F6=RMFHelp    F9=SwapScr
 F12=Return
```

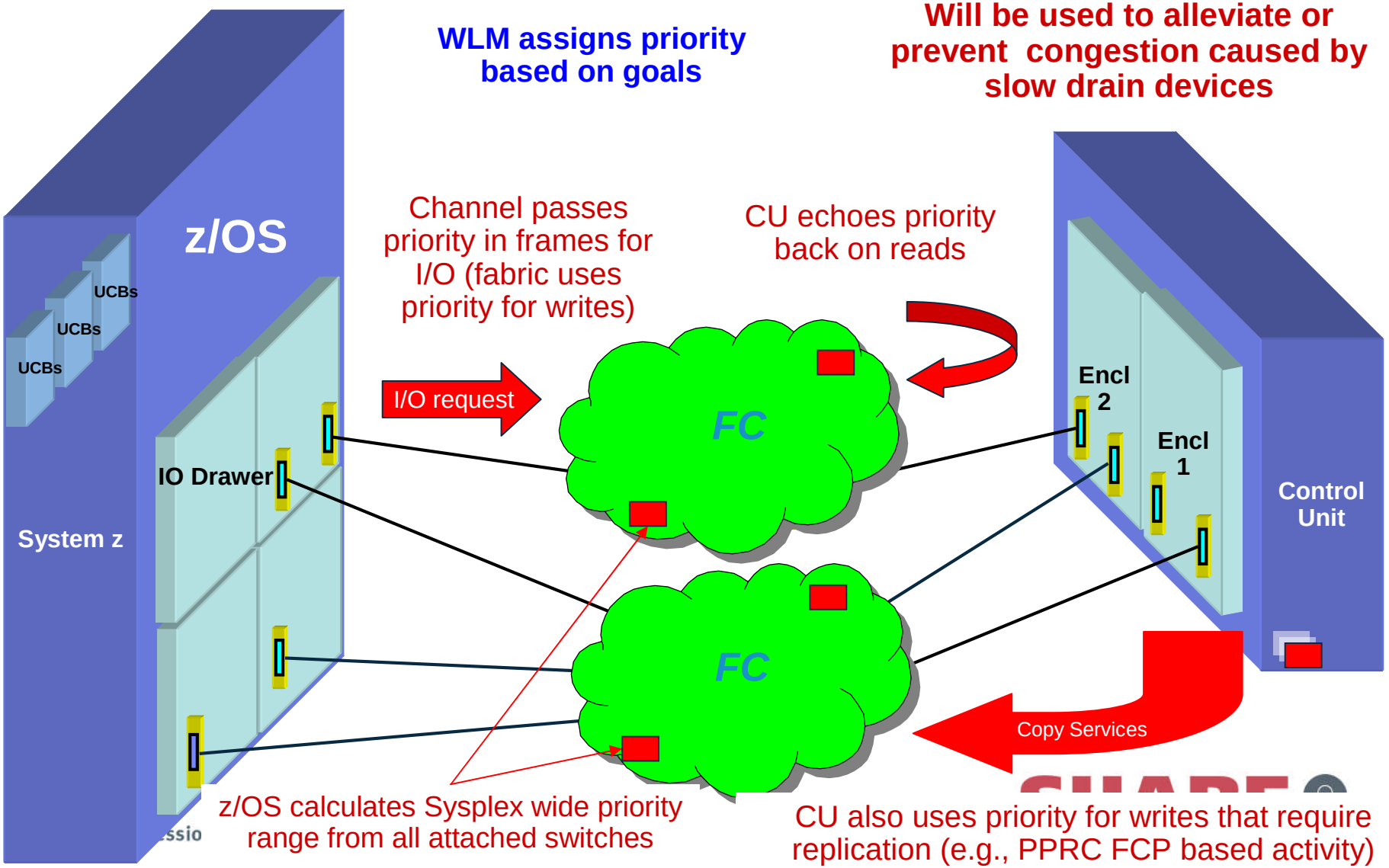
Increase number of coupling links from 128 to 256 per CEC

- **z13 now supports 256 Links (planned availability June 26, 2015)**
  - A single z/OS or CF image supports a maximum of 128 Links
    - Enabling enhanced connectivity and scalability for continued sysplex growth
    - Increased capabilities to consolidate multiple sysplexes into the same set of physical servers
- **When displaying STP (D ETR) from a z/OS image, information is provided for the entire CEC**
- **If >128 links are defined on z13**
  - z/OS uses CHSC STP commands to retrieve information about coupling links (which are used for timing signals).
  - The z/OS support (or toleration) must be installed on all z/OS releases running on z13
    - Allowing STP information to display > 128 links STP information

4th Subchannel Set Exploitation Considerations

- **You can now define a 4th subchannel set, which gives you addressability to another 64K subchannels/devices.**
  - **These subchannels can be used for either PAV alias devices, PPRC secondary devices, or FlashCopy target devices.**
- **If you need to fall back (hardware or software), then**
  - You will lose access to the devices in the 4th subchannel set,
    - Which means these devices must be defined in older I/O configuration in the remaining 3 subchannel sets.
    - Otherwise, you may experience performance problems (e.g., not enough available PAV alias devices) or lose hyperswap capability (if PPRC secondary devices are in the 4th subchannel set). To avoid this problem you should
      - move devices out of another subchannel set into the new one, and then do sufficient testing before reusing the older device numbers for other uses (i.e., for additional primary devices).
      - Separate OSCONFIG for lower servers w/o Subchannel set 3

Fabric I/O Priority for an I/O request …



Fabric Priority for an I/O request

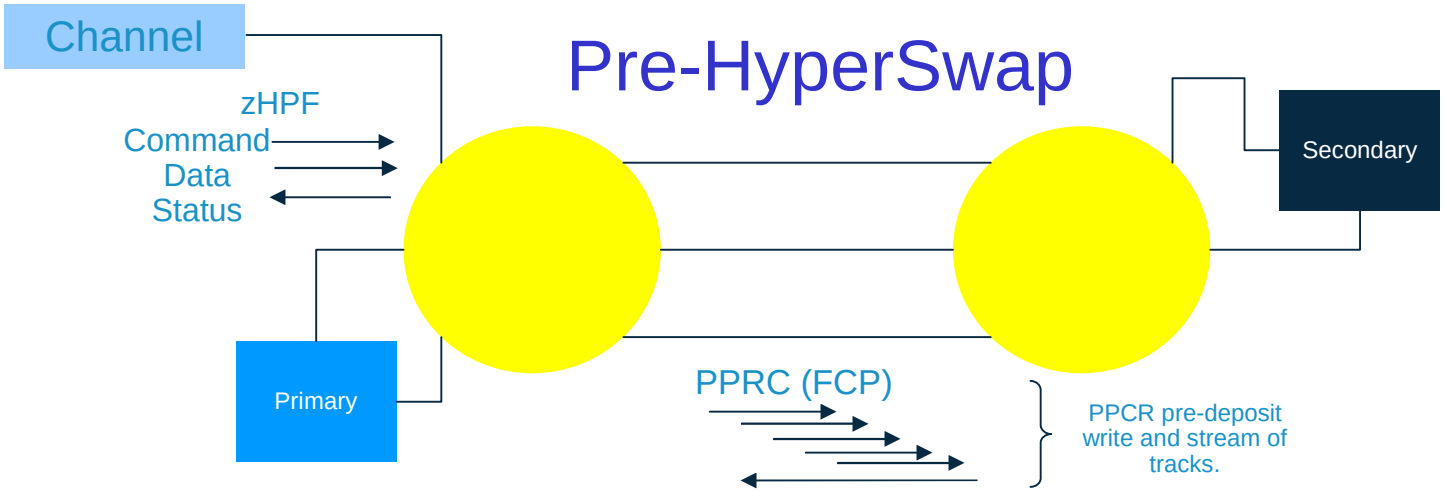
- **Planned availability September 25, 2015* (APAR OA47297)**
- **Provide the ability for z/OS to pass a fabric priority for an I/O request.**
  - The fabric priority is used when the processor is connected to the devices via one or more FICON switches or directors.
  - The fabric priority is used by the switch when congestion occurs to determine which I/O requests should be given preference.
- **The fabric priority range to be used is obtained by z/OS from the control unit port (CUP) device associated with the switch.**
  - The information returned contains the maximum priority used by the switch (the minimum is assumed to be 1).
  - This global maximum priority is used by WLM to assign a fabric priority to an address space or enclave based on the performance goals of the unit of work.
  - IOS extracts the priority assigned by WLM and passes it to the channel subsystem when the I/O is started if WLM's Service Definition the function for I/O Priority Management is set active.
  - The channel that is selected adds the fabric priority to each of the frames associated with the I/O request, which can then be used by the switch to prioritize the frames.

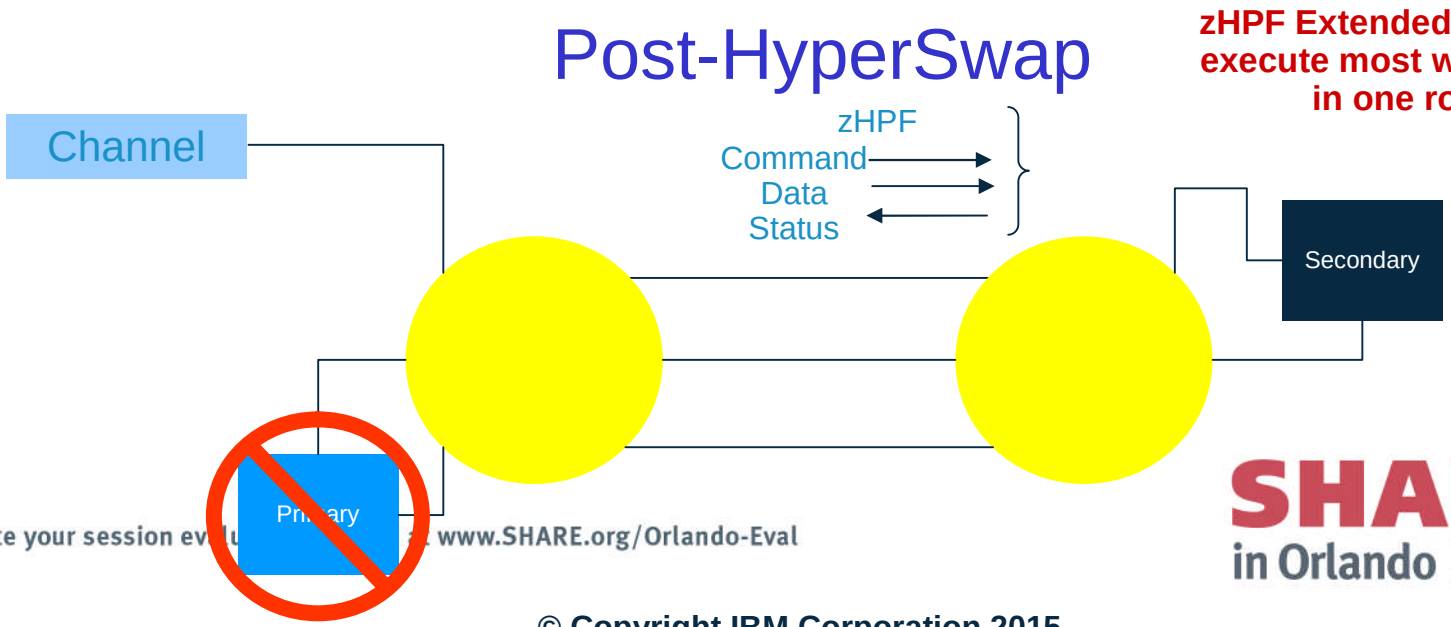
* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

Fabric Priority for an I/O request …

- **To enable the function you must:**
  - Install the firmware on the switch that supports the Control Unit Port (CUP) function,
  - Define the switches as z/OS devices in the IODF, and
  - Bring them online.
    - This allows z/OS to obtain the maximum priority for the switch.
  - DS8000 and TS7700 microcode should be installed that echoes the priority in the frames for read I/O requests.
  - Set I/O Priority Management active in your WLM Service Definition
  - IECIOSxx or SETIOS FICON,FABRICPRTY=YES|NO can be used to enable or disable the function.
    - The default is YES (enable).

Improved zHPF I/O Execution at Distance



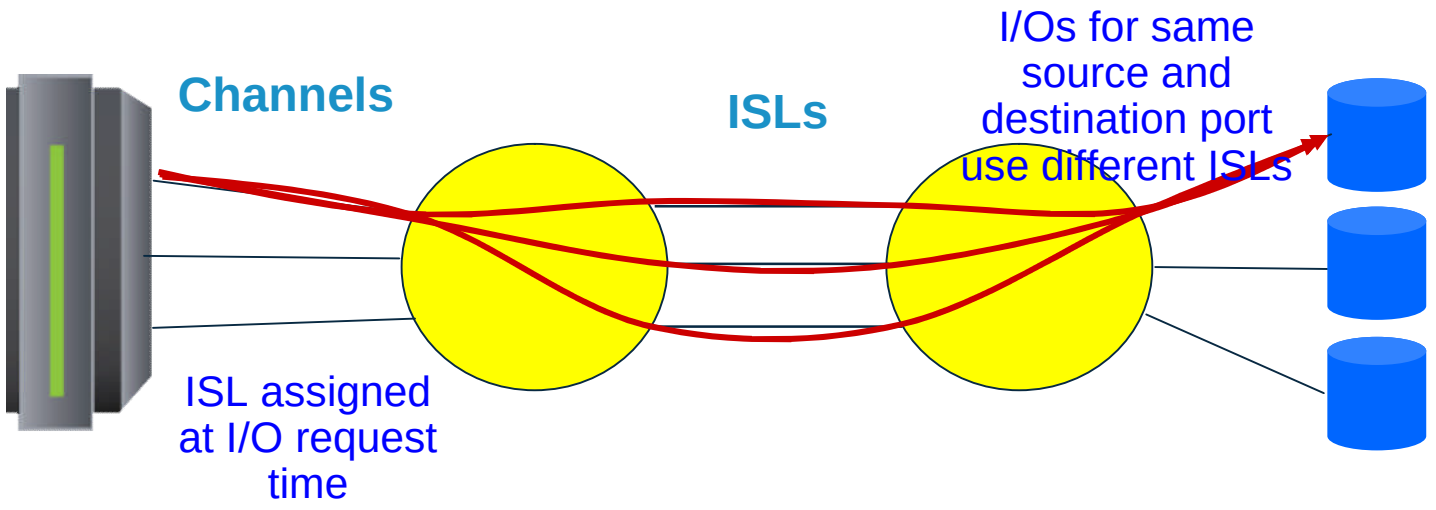


Improved zHPF I/O Execution at Distance …

Available since June 30, 2015

- RMF Monitor I & II data gatherers are enhanced to request new Format-2 Secondary-Queue Measurement blocks whenever the Store-Channel-Subsystem Characteristics response block indicates that the extended I/O-measurement-block-2 facility is installed
- The I/O Queuing configuration data sections of SMF record 78 subtype 3 and SMF record 79 subtype 14 are extended to provide new transport-mode related performance counters for each configured CHPID
  - transport-mode-write-count
  - first-transfer-ready-disabled write count
- First-transfer-ready-disabled inhibited ratio is reported through new RMF Postprocessor Overview condition

Dynamic Routing (Exchange Based Routing, OxID)



- Dynamic Routing (Brocade EBR or CISCO OxID) dynamically changes the routing between the channel and control unit based on the “Fibre Channel Exchange ID”
- Each I/O operation has a unique exchange id
- Client Value:
  - **Reduces cost by allowing sharing of ISLs between FICON, FCP (PPRC or distributed)**
  - I/O traffic is better balanced between all available ISLs
  - Improves utilization of switch and ISL hardware – ~37.5% bandwidth increase
  - Easier to manage
  - Easier to do capacity planning for ISL bandwidth requirements
  - Predictable, repeatable I/O performance
  - Positions FICON for future technology improvements, such as work load based routing

Manage FICON Dynamic Routing

- **Planned availability September 25, 2015***
  - New FICON Dynamic Routing lowers client costs, improve performance and resilience by incorporating the pervasive SAN dynamic routing policies supported by switch vendors.
    - Businesses can experience simplified configuration and capacity planning as it pertains to network performance and utilization through the use of FICON Dynamic Routing.
- **Planned availability 4Q2015***
  - HCD/HCM assists clients from accidentally defining a dynamic routing device to a fabric, which is not capable of dynamic routing.
    - A new dynamic routing attribute will be added to switches and control units, which can be considered in the HCD/HCM dialogs.
      - Based on this flag HCD will perform a check at build production IODF, whether dynamic routing is supported on the complete path.
      - A warning message will be shown, if a mixture of dynamic routing capable and incapable control units and switches is found.
  - HCD will allow users to split configurations to be FICON Dynamic Routing capable and FICON Dynamic Routing incapable

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

Manage FICON Dynamic Routing …

- **To enable FICON Dynamic Routing you must:**
  - Install the firmware on the switch that supports the Control Unit Port (CUP) function,
  - Install exploitation support and toleration support on all systems updating an IODF with FICON Dynamic Routing definitions
  - Install UIM updates to enable FICON Dynamic Routing
    - The UIMs are needed to allow HCD to define and verify Dynamic Routing definitions
  - Define FICON Dynamic Routing capability via HCD/HCM
  - Bring them online.

Health Check for FICON Dynamic Routing

- **Planned availability September 25, 2015* (APAR OA47297)**
- **z13 is changing the channel microcode to support dynamic routing.**
  - No changes are needed in z/OS to support dynamic routing.
  - However, if a customer configures their switches for dynamic routing and either the processor and/or storage controllers do not support it, then this can lead to I/O errors.
    - Therefore, a health check is being provided that interrogates the switch to determine if dynamic routing is enabled in the switch fabric.
      - If so, then the dynamic routing capability of the processor and control units is checked.
      - If either do not support dynamic routing, then a health check exception is surfaced.
      - Running the health check in VERBOSE(YES) mode will cause the health check to check whether all devices support dynamic routing, regardless of whether the devices are connected to a switch fabric that is enabled for dynamic routing.
        - » This allows the customer to plan for enabling dynamic routing since changing the routing policy is disruptive to the switch.
      - The health check is applicable to all processors.
        - » That is, if you enable dynamic routing in the switch fabric connected to a non-z13 processor, this health check will report an exception since I/O errors may occur.

Health Check for FICON Dynamic Routing …

- **No action is required to enable the health check.**
  - It will automatically be enabled at IPL and react to changes that might cause problems. For example:
    - Varying on the first device for a control unit that does not support dynamic routing, when the control unit is connected to a switch fabric enabled for dynamic routing
    - Configuring a new channel online that is connected to a switch fabric enabled for dynamic routing
  - The health check can be disabled via modify commands, PARMLIB or via SDSF

Crypto Express5S Considerations

- **Crypto Express5S Toleration**
  - Toleration PTFs are required to treat Crypto Express5S as Crypto Express4S

z/OS 1.13+

- **Crypto Express5S Exploitation (software installation)**
  - ***Enhanced Cryptographic Support for z/OS V1.13 and z/OS V2.1*** web deliverable (HCR77B0)
    - ***NOT*** integrated in z/OS V2.1 ServerPac or CBPDO orders
    - Planned to be integrated into z/OS V2.2 ServerPac or CBPDO orders
    - Only needed for the following hardware or software functions
      - Next Generation Coprocessor support and Format Preserving Encryption (FPE)

ICSF New Function PTFs (SPEs)

- **DK AES PIN Phase 4 (June 26, 2015 – APAR OA46466)**
  - Provides additional Common Cryptographic Architecture (CCA) support for German Banking Industry-defined PIN processing functions.
  - These functions include three types of AES key derivation as well as AES Secure Messaging Keys, which can be used in AES-based EMV transactions.
    - This support requires a minimum microcode level (MCL) for Crypto Express4S and Crypto Express5S coprocessors on EC12 and later processors.
    - Available on HCR77A0 and higher
- **EMV Simplification (July 2015 – APAR OA47016)**
  - Introduces six new EMV-centric ICSF services intended to simplify EMV payment processing.
    - Available on HCR77A0 and higher
- **CCA Verb Algorithm Currency Part A (Planned for August 2015 – APAR OA47781)***
  - Provides additional Common Cryptographic Architecture (CCA) support for generation of a single key for the CIPHER, DATAC, and DATAM key types.
  - Support is also planned for RSA-OAEP block formatting for both SHA-1 and SHA-256 hashing in the PKA Encrypt (CSNDPKE) and PKA Decrypt (CSNDPKD) callable services.
  - ICSF will be designed to format returned data using the RSAES-OAEP encryption/decryption scheme defined in the RSA PKCS #1 v2.0 standard.
    - This support requires a minimum MCL for Crypto Express4S and Crypto Express5S coprocessors on EC12 and later processors.
    - Available on HCR77A0 and higher

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

Crypto Express5S Coexistence and Migration Considerations

- **Support architecture for up to 85 Domains**
  - If an ICSF release supporting 85 Domains is run on older hardware (e.g. zEC12) and specifies a domain greater than 15 in the Installation Options Data Set, ICSF will return error message.
    - If the Installation Options Data Set indicates a domain, it should not be shared across ICSF instances.
- **"Inherited" migration actions for the following functions:**
  - AP Configuration simplification
  - CCF Removal
  - CTRACE Enhancements
  - KDS Key Utilization Stats – only if implemented
  - UDX (User Defined eXtension)
- **PTFs that allow prior levels of ICSF to coexist with, and fallback from, the Enhanced Cryptographic Support for z/OS V1.13 and z/OS V2.1 web deliverable**
  - IBM.Coexistence.ICSF.z/OS_V1R13-V2R1-HCR77B0

Two-way simultaneous multithreaded (SMT) operation

- **Support provided for IFL and zIIP**
- **Increased capacity**
  - Achieved through increased parallelism
  - Twice as many execution paths as similarly configured zEC12
- **No application changes required to exploit MT**
  - Automatic upgrade
- **Comprehensive measurement data for performance monitoring, capacity planning, accounting, and chargeback**
- **Optional enablement for each z/OS, z/VM, or zLinux instance**

Simultaneous multithreaded (SMT) operation

- New LOADxx PARMLIB controls to define a PROCessor VIEW of CORE|CPU for the life of the IPL.
  - **PROCVIEW CORE on z13 enables MT support**
    - Becomes MT-2 configuration, allocates 2 threads per core
    - Forces IEAOPTxx HiperDispatch=YES
    - Requires ConFig Core, Display Matrix=Core commands
    - PROCVIEW CORE can be specified on all servers to manage the environment using MT controls
      - (Config Core, Display Matrix=Core, etc)
    - PROCVIEW CORE,CPU_OK causes z/OS to treat CPU as an acceptable alias for CORE
  - **PROCVIEW CPU can be specified on all servers but results in the existing function and management controls**
    - Establishes existing (Pre-MT, MT-1) environment, uses Pre-MT command controls
      - Retains MT-1 configuration, allocates 1 CPU per core
      - Requires ConFig CPU, Display Matrix=CPU commands
  - **Fallback from PROCVIEW CORE to PROCVIEW CPU requires reIPL**

Simultaneous multithreaded (SMT) operation …

- **New IEAOPTxx parameter to control zIIP MT Mode**
  - Without an IPL you can change the zIIP processor class MT Mode (the number of active threads per online zIIP) using IEAOPTxx
  - MT_ZIIP_MODE=2 (MT_ZIIP_MODE=1)
    - MT_ZIIP_MODE=2 for 2 active threads (the default is 1)
    - When PROCVIEW CPU is specified the processor class MT Mode is always 1
    - PROCVIEW CPU, and PROCVIEW CORE MT Mode=1 receive the same performance

  Note: CP cores always use MT Mode=1
- **New LOADxx and IEAOPTxx controls ONLY available on z/OS V2.1 and higher**
  - Requires a separate LOADxx for z/OS V1.13 or z/OS V1.12 if SMT is exploited

Miscellaneous PCIe Enhancements

- **The following PCIe enhancements are planned:**
  1. **PCIe extended address translation**
  2. **Greater than 256 PFID support**
  3. **Add PCIe function type to the PCIe function definition in the I/O configuration**
  4. **PCIe function measurement block changes**

PCIe Extended Address Translation

z/OS 2.1

- **PCIe adapters like RoCE and zEDC use a direct memory access (DMA) protocol to access System z storage.**
- **The translation of the DMA address to the real storage address is done under the control of the zIOC chip, which is between the PCIe card in the I/O drawer and the processor book.**
  - The zIOC chip has a translation look-aside buffer (TLB) to cache translation results similar to the TLB used by the CPUs. If the adapter needs to access a DMA address whose page table entry is not in the TLB, then the page table entry must be fetched from memory.
- **In z/OS, five 1MB pages are set aside to create the DMA table.**
  - One page is used as the region table which points to 4 page tables, which then point to the individual 4K pages in z/OS memory.
  - This allows up to 2GB of 4K pages to be addressed by the PCIe card.
- **With z13, the zIOC function is being moved to the processor book, which means that space for caching translation results is even more limited.**
  - z/OS will now define a single level page table that consists of up to 64K contiguous 1MB pages.
    - This means that only one address needs to be cached to resolve DMA address translations.
- **RMF can be used to report the benefit of the PCIe extended address translation line item.**
  - Throughput should be improved when a large number of adapters and transactions are in progress.

Support for More than 256 PFIDs

- **On the zEC12 and zBC12 processors, the maximum number of PCIe function ids (PFIDs) is limited to 256, primarily because z/OS provided support only for a single digit PFID in commands and messages. This was sufficient since the maximum number of PFIDs that could be defined on the zEC12 was less than 256. This consisted of the following:**
  - Up to 16 RoCE cards. Each RoCE card can only be used by a single LPAR (no virtual function support), so only 16 PFIDs are used.
  - Up to 8 zEDC cards that can be shared by up to 15 LPARs (up to 15 virtual functions can be defined per card), so 8 * 15 PFIDs are used.
- **For z13, each of the 16 RoCE cards may be shared by up to 31 LPARs each, so more than 256 PFIDs are now required.**
- **The following changes are being made:**
  - Reconfiguration and display commands involving PFIDs will be changed to support an 8 digit PFID (this is the architectural maximum)
  - PCIe related messages will be changed to display 8 digit PFIDs.
    - The H/W accelerator manager (HWAM) component messages do not need to be changed, since they already display 8 digit PFIDs
  - PCIe is changed to allow more than 256 devices to be defined in its internal tables.

Add Function Type to PCIe Function Definition

- **Add PCIe function type (PFT) to the PCIe function definition in the IODF/IOCDS**
  - Identifies the type of PCIe function represented by the adapter (RoCE, zEDC, etc.).
  - This will be used by the System z firmware to validate that the PCIe device plugged into the I/O drawer is the one defined in the I/O configuration.
  - This function currently exists for channels, but did not exist for PCIe devices.
- **The PCIe function type used by HCD and defined in the IODF is now also considered by IOS and the IOCP program.**
  - It is passed to IOS when activating a new production IODF, and added to the input decks passed to the IOCP program used to build an IOCDS.
  - IOS is changed to pass this information to the channel subsystem when adding new PCIe function as a result of a dynamic activate.

Function Measurement Block Changes

- **A function measurement block (FMB) is assigned by the OS when a PCIe device is allocated.**
  - It contains PCIe related statistics (e.g., number of PCI loads and stores) that are reported by the IQPINFO macro.
  - RMF uses this macro to collect information for the PCIe function report.
- **In z13, the FMB is being extended to report function specific statistics for zEDC and RoCE devices.**
  - The measurement block has different formats depending on the PCI function type (RoCE devices or zEDC devices)
    - A new format field is provided to indicate which data is present.
- **PCIe will be changed to ensure that the correct size measurement block is allocated based on the PCIe function type.**
- **RMF changed is to report the new PCIe statistics**

SMC-R (10GbE RoCE Express) Single root (I/O virtualization)

- **Shared RoCE Support provides the following benefits:**
  - The ability to concurrently share the same physical adapter (PCHID) with up to 31 LPARs.
  - The capability to concurrently use both 10GbE ports on the same adapter
    - With dedicated support (zEC12 GA2 functionality) z/OS could only use 1 physical port.
- **To exploit you must:**
  - Define Virtual Functions (VF) in IOCDS via HCD/HCM
  - Have a unique Function ID (FID) defined for each VF
  - If you use Communications Server multi-stack (per z/OS instance), you would need to alter your TCP/IP profile.
    - No changes to single stack as long as FID was not changed.
- **SMC Applicability Tool:**
  - Identifies the amount of traffic that would benefit and if any CPU savings would be gained from using SMC-R versus TCP/IP

Exploitation of XL C/C++ ARCH(11) and TUNE(11)

z/OS 2.1+

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- **Unlike prior generations of servers, exploitation of new hardware instructions using XL C/C++ ARCH(11) and TUNE(11) or SIMD exploitation by MASS and ATLAS Libraries, requires the *XL C/C++ V2R1M1 web deliverable with z13 support for z/OS 2.1* web deliverable**
- The web deliverable contains the following enhancements:
  - ARCH(11)/TUNE(11) compiler options
  - SIMD/vector support
    - Vector infrastructure – datatypes, options, linkages – for language support
    - Over 300 built-in functions for storage access, integer intrinsics, string intrinsics, floating point intrinsics and infix operations
    - Vector debug support (generation of dwarf debug information consumable by debuggers)
  - New z13 hardware instruction support
    - LOAD HALFWORD HIGH IMMEDIATE ON CONDITION
    - LOAD HALFWORD IMMEDIATE ON CONDITION
    - LOAD HIGH ON CONDITION
    - STORE HIGH ON CONDITION
  - Decimal Floating Point packed conversion facility support
  - Performance improvements

Exploitation of XL C/C++ ARCH(11) and TUNE(11)

- **C/C++ ARCH(11) and TUNE(11) options:**
  - The ARCHITECTURE C/C++ compiler option selects the minimum level of machine architecture on which your program will run.
    - ARCH(11) exploits instructions available on a z13 server
    - The TUNE compiler option allows you to optimize your application for a specific machine architecture within the constraints imposed by the ARCHITECTURE option
      - The TUNE level has to be at least the ARCH level
      - If the TUNE level is lower than the specified ARCH level, the compiler forces TUNE to match the ARCH level or uses the default TUNE level, whichever is greater.
      - For more information on the ARCHITECTURE and TUNE compiler options refer to the z/OS XL C/C++ User's Guide.
- **Exploitation Restriction:**
  - Code compiled with the C/C++ ARCH(11) option can only run on z13 servers, otherwise an operation exception will result
  - This is a consideration for programs running on different level servers during development, test, production, and during fallback or DR

Exploitation of XL C/C++ ARCH(11) and TUNE(11)

- **Please note the following restrictions:**
  - Mixing context switching between ARCH(11) and pre-ARCH(11) code will not work due to SETJMP and LONGJMP changes.
    - If you are setting a context or jump buffer in one CU and trying to jump to it in another one, and one of the CU's is ARCH 11 and the other less than that, then the jump buffer sizes will be different and you will have a binary incompatibility.
    - Generally the CU's will be compiled together at the same ARCH level so this should not be a problem, but code should be scanned for any unpaired setjmp/longjmp C runtime function calls.
  - C/C++ applications that use FP registers (0-15) and vector registers (1-7) needs to be recompiled so that all modules/binaries are at the same level.
    - Applications that use GP registers will continue to work unchanged.
    - Users can verify if they're using FP and vector registers by checking to see if the VECTOR option is being used as this option allows vector register usage by the compiler, checking to see if any code uses floating point calculations or checking the psuedo assembly listing
  - Metal C (non-LE) users who write their own prolog/epilogs need to save and restore FPR/VR's if overlaid vector registers are used

Single Instruction Multiple Data (SIMD) instruction set and execution

z/OS Support includes the following:

- Enablement of Vector Registers (VR)
- Use of VR when using XL C/C++ ARCH(11) and TUNE(11)
- MASS – Mathematical Acceleration Sub-System
  - A math library with optimized and tuned math functions
  - Has SIMD, vectorized, and non-vectorized version
  - Can be used in place of some of the C Standard math functions
- ATLAS (Automatically Tuned Linear Algebra Software)
  - A specialized math library that is optimized for the hardware
- LE enablement for ATLAS (for C runtime functions)
- DBX to support disassemble the new vector instructions, and to display and set vector registers
- XML SS Exploitation to use new vector processing instructions to improve the performance
- IBM 31-bit SDK for z/OS, Java Technology Edition, Version 8 and IBM 64-bit SDK for z/OS, Java Technology Edition, Version 8
- Enterprise PL/I for z/OS, V4.5
- Enterprise COBOL for z/OS, V5.2

SIMD Exploitation Considerations

- **MASS Libraries**
  - The z13 libraries require SIMD instruction support for the SIMD and vector version of MASS.
  - The scalar version of the library does not use SIMD instructions
  - The zEC12 libraries (vector and scalar) do not use SIMD instructions
- **ATLAS Libraries**
  - ATLAS has a version for z13 and another version for zEC12
- **Either Library**
  - Any library function calls will abend if run on a lower hardware level system
  - Any z13 library function calls will abend if run on pre-z13 generation server
  - Therefore don't use the z13 version of the MASS and ATLAS libraries until the compiled application is targeted to run on an z13 server
- **XL C/C++ Performance Improvements can be measured using Performance Analyzer**

SIMD Exploitation Considerations

- **To use the MASS library functions instead of the standard math library functions, the MASS library must be put first in the library concatenation**
  - The xlc.cfg stanza's can be modified to put the MASS library first in the sysobj attribute
  - The compiler procs can be modified to put the MASS library first in the SYSOBJ DD concatenation
- **To use the libraries alongside the standard math library, the libraries can be added to the end of the library concatenation**
  - This means that the MASS functions that are common with the C standard library will not be used
- **POSIX(ON) is required for ATLAS to run in multi-threaded mode for maximum performance**

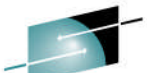
SIMD Migration, and Fallback Considerations

- **This is new functionality and code will have to be created to take advantage of it**
- **Some math function replacement can be done without code changes by inclusion of the scalar MASS library before the standard math library**
  - Different accuracy for MASS vs. the standard math library
  - IEEE is the only mode allowed for MASS
    - Rounding mode must be to nearest and exceptions must be masked
  - Overlap of arguments may result in undefined behavior in MASS
  - Migration Action: Assess the accuracy of the functions in the context of the user application when deciding whether to use the MASS and ATLAS libraries.
- **LOADxx MACHMIG can be used to disable SIMD at IPL time**

Agenda

- IBM z13 Overview
- z/OS Support by Release
- Hardware PSP Buckets and Fix Categories
- Migration Considerations
  - General
  - z13 Migration Considerations
  - Sysplex and Multisystem Considerations
  - Exploitation Considerations for Selected Functions
- **Summary**
- Backup

Summary of z/OS Support for z13



- **Provides same functionality as that on the IBM zEC12 plus**
- **z/OS V1.12**
  - **FICON Express16S**
  - **Greater than 128 Coupling Links toleration**
  - **Crypto Express5S toleration**
    - **Treats Crypto Express5S as Crypto Express4S**
  - **Support architecture for up to 85 Domains on Crypto Express4S and Crypto Express5S**
  - **New z/Architecture Instructions (assembler new OPCODE support)**
- **z/OS V1.13**
  - **Changed (node) cache structure optimized by HiperDispatch**
  - **Greater than 128 Coupling Links per CEC**
  - **CF Level 20 support**
  - **Integrated Coupling Adapter (ICA) Links**
  - **Crypto Express5S exploitation (if web deliverable is installed)**
    - **Next Generation Coprocessor support, Format Preserving Encryption (FPE)**
  - **Improved Channel Subsystem Scalability**
    - **Up to 85 LPARs**
      - Only up to 60 LPARs can be defined if z/OS V1.12 is running in one of the LPARs
    - **Up to six logical channel subsystems (CSSs)**
    - **4 Subchannel Sets per CSS**
  - **Improved zHPF I/O Execution at Distance**
  - **Manage FICON Dynamic Routing**
  - **Fabric Priority for an I/O request**
- **z/OS V2.1**
  - **Shared RoCE Support**
  - **Two-way simultaneous multithreaded (SMT) operation**
  - **Up to 141-way in non-SMT mode (up to 128 way in SMT mode)**
  - **Increase number of coupling links from 128 to 256 (STP)**
  - **Health Check for FICON Dynamic Routing**
  - **Miscellaneous PCIe enhancements**
    - **PCIe extended address translation**
    - **Greater than 256 PFID support**
    - **Add PCIe function type to the PCIe function definition in the I/O configuration**
    - **PCIe function measurement block changes**
  - **Single Instruction Multiple Data (SIMD) instruction set and execution: Business Analytics Vector Processing**
    - **MASS and ATLAS Library, SPSS Modeler and ILOG Cplex**
  - **Exploitation of new hardware instructions – XL C/C++ ARCH(11) and TUNE(11)**
    - **New z13 hardware instruction support**
    - **SIMD (Vector support) and Vector data**
    - **Decimal Floating Point packed conversion facility support**
    - **Performance improvements**
      - Machine model scheduling and code generation updates
  - **Up to 4 TB per z/OS LPAR (statement of direction)**

z/OS Support Summary

Release	IBM.Device.Server.z13-2964.RequiredService										IBM.Device.Server.z13-2964.Exploitation																							
	Base Support	CPU Measurement Facility	Crypto Express5S Toleration	FICON Express 8S	FICON Express 16S	z13 Assembler Support	OSA-Express4S	OSA-Express5S	GRS Support for FICON CTCs	High Performance FICON (zHPF)	InfiniBand Coupling Links	Support for 256 Coupling Links/CEC	>16 Cryptographic Domains	CF Level 20 Support	Integrated Coupling Links (ICA SR)	SAN Fabric I/O Priority	FICON Dynamic Routing	Improved CSS Scalability	zAware	Transactional Memory	Improved zHPF I/O Execution at Distance	zEnterprise Data Compression (zEDC)	Flash Express	2GB Large Pages	Crypto Express5S Exploitation	Shared ROCE Express Support	Simultaneous Multithreading (SMT)	Miscellaneous PCIe Enhancements	Greater than 100 CPs per z/OS Image[3]	Single Instruction Multiple Data (SIMD)	z13 XL C/C++ Support	Up to 4TB per z/OS LPAR
z/OS V1.12[1]	Y	Y	W	Y	Y	Y	Y	Y	Y	Y	Y	T	W									T										
z/OS V1.13	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	T	W	W	W							
z/OS V2.1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	W	Y	Y	Y	Y	Y	W	Y[4]
z/OS 2.2[2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Notes:

1 Beginning with z/OS V1.12, IBM Software Support Services replaces the IBM Lifecycle Extension for z/OS offering with a service extension for extended defect support.

2 Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

3 Up to 141-way in non-SMT mode (up to 128-way in SMT mode)

4 Up to 4TB per z/OS is a statement of direction for z/OS V2.1

T Coexistence support provided

W A web deliverable is required for exploitation support available at http://www-03.ibm.com/systems/z/os/zos/downloads/

Summary of z/OS Support for z13

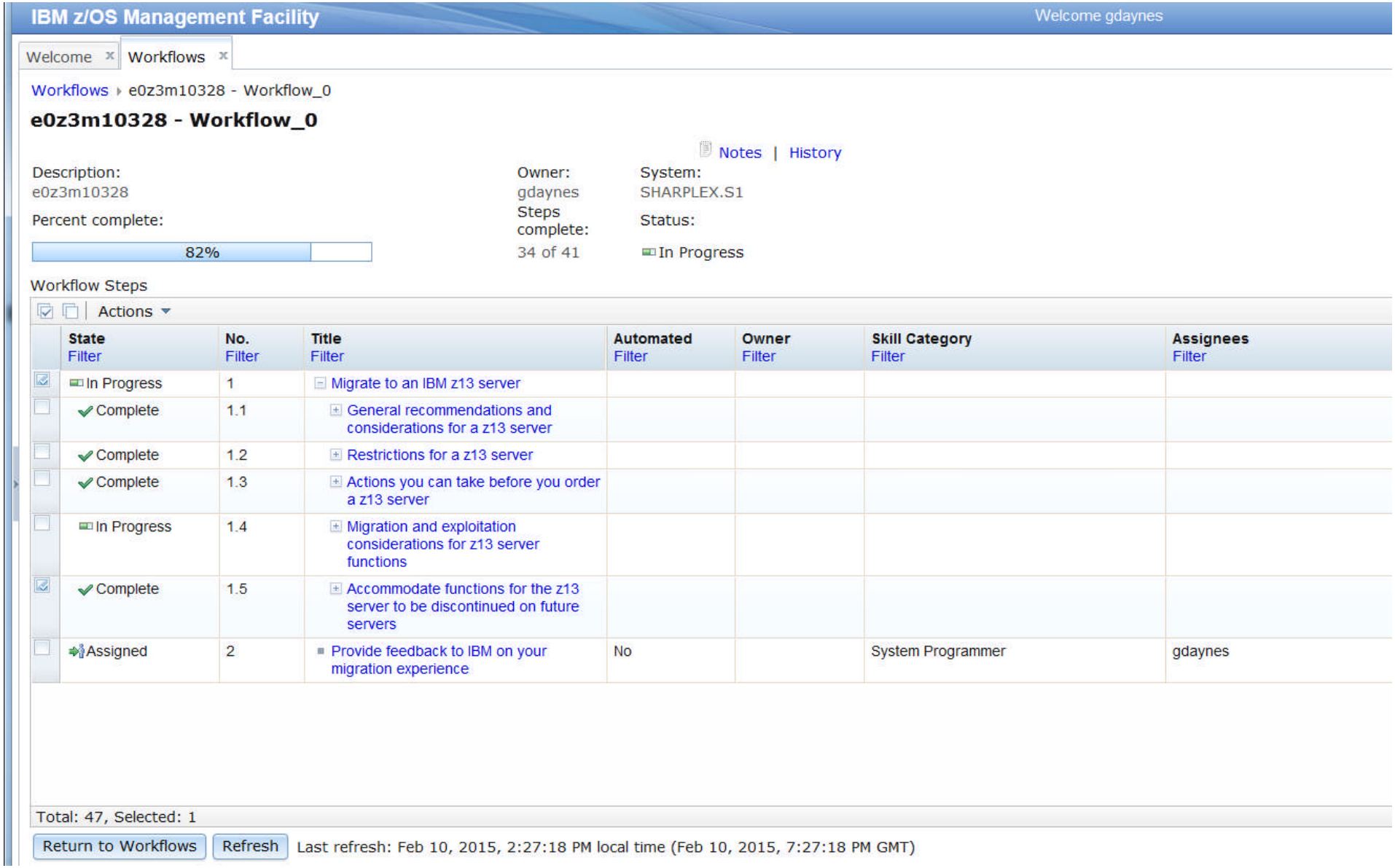
- **Base support is provided by PTFs identified by:**
  - **IBM.Device.Server.z13-2964.RequiredService**
- **Exploitation of many functions is provided by PTFs identified by:**
  - **IBM.Device.Server.z13-2964.Exploitation**
- **Recommended service is identified by:**
  - **IBM.Device.Server.z13-2964.RecommendedService**
    - Should also be either “required service” or “exploitation”
- **Exploitation of some functions requires a web deliverable**
  - Exploitation of Crypto Express5S requires the ***Enhanced Cryptographic Support for z/OS V1.13 and z/OS V2.1*** web deliverable
  - Exploitation of new hardware instructions using XL C/C++ ARCH(11) and TUNE(11) or SIMD exploitation by MASS and ATLAS Libraries, requires the ***XL C/C++ V2R1M1 web deliverable with z13 support for z/OS 2.1*** web deliverable
  - Exploitation of Flash Express or 2GB Large pages on z/OS V1.13 requires the **z/OS V1.13 RSM Enablement** web deliverable
- **All support is planned to be included in the z/OS V2.2* base**

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

NEW: z/OSMF Workflow Support

- **All the z/OS considerations contained in this presentation are documented in the *z/OS V2.1 Migration* book (-03 level, or later)**
- **The z13 topics from the *z/OS V2.1 Migration* book have been put into a z/OSMF Workflow!!!**
  - z/OSMF V2.1 users can download the workflow and use it to track their z/OS upgrade required to support the z13
    - http://www-03.ibm.com/systems/z/os/zos/tools/downloads/zosmf-z13-migration-workflow.html
  - Users are encouraged to provide feedback on the Workflow
    - Just complete the last set in the Workflow

IBM z13 Server Migration Workflow



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Crypto HCR77A1 Migration Considerations (1 of 5)

- **Installation of the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable introduces the following considerations:**
  - **Adjunct Processors (AP) Configuration simplification**
    - The new Adjunct Processors (AP) configuration processing will compare each master key verification pattern (MKVPs) present in the CKDS/PKDS or TKDS to the corresponding MKVP for a given processor, if supported by that processor. If any do not match, the processor will not become active and available for work.
      - In previous releases, if a subset of the master keys matched, the coprocessor could become active.
      - A migration health check ICSFMIG77A1_COPROCESSOR_ACTIVE will be implemented for HCR7770, HCR7780, HCR7790 and HCR77A0. The health check warns the user when master key configuration of crypto devices does not match the active key data stores which could result in crypto devices not being activated after migration to HCR77A1.

Crypto HCR77A1 Migration Considerations (2 of 5)

- **Installation of the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable introduces the following considerations:**
  - **CCF Removal (removes support for the z800 and z900 machines)**
    - Migration actions are required by the user to accommodate this change due to:
      - Removal of services which are no longer supported by the hardware
      - Removal of BHAPI support
      - Removal/renaming of field names
      - The DATAXLAT key type is no longer supported (KGN, SKI, or KGUP) requires CCF system.
    - A migration check ICSFMIG77A1_UNSUPPORTED_HW will be created to check that the current hardware will be able to start ICSF FMID HCR77A1. If not, the migration check will indicate that HCR77A1 will not be able to start. The message will be:
      - **CSFH0017I Processor will not be supported by ICSF after migration**
    - In addition, any customer that has z800/z900 servers and zEC12/zBC12 (with the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable installed, will need to maintain 2 software stacks
      1. One with the level of ICSF prior to the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable
      2. One with the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable installed

Crypto HCR77A1 Migration Considerations (3 of 5)

- **Installation of the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable introduces the following considerations:**
  - **CTRACE Enhancements**
    - Previously, ICSF supported the TRACEENTRY option in the Options dataset, which allowed the user to configure the maximum number of CTRACE records in the ICSF buffer.
      - This option is deprecated, but will not prevent ICSF initialization.
    - Now, ICSF supports the CTRACE(CTICSFxx) option in the Options dataset, which provides the name of a PARMLIB member containing ICSF's CTRACE options.
    - **No action is required to take advantage of this new function.**
      - If the TRACEENTRY option is present, it will merely cause a JOBLOG message (CSFO0212) and the value will be ignored.
      - If the CTRACE option is not present, ICSF will behave as if CTRACE(CTICSF00) was specified.
        - » If the PARMLIB member specified (or CTICSF00 if defaulted) is not present, ICSF will select a reasonable set of options (the same options present in the CTICSF00 sample installed via SMP/E).
      - The TRACEENTRY option can remain in the Options dataset, especially if it is shared across multiple ICSF instances.
        - » The presence of the option will not adversely affect HCR77A1.
        - » Additionally, the CTRACE option can be added and bracketed with BEGIN(HCR77A1)/END if settings other than the defaults in CTICSF00 are desired on HCR77A1 systems.

Crypto HCR77A1 Migration Considerations (4 of 5)

- **Installation of the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable introduces the following considerations:**
  - **KDS Key Utilization Stats – only if implemented**
    - **KDS Key Utilization Stats will introduce a new format of KDS records.**
    - The Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable is compatible with old versions of the KDS. Only the TKDS is affected incompatibly.
      - The web deliverable will support a new format of KDS records.
      - It will be compatible with old versions of the KDS.
      - There will be a utility to migrate a KDS in the old format to the new format.
        - » Once in the new format a KDS cannot be converted back to the earlier format.
      - Prior releases will not be able to run with a KDS in the new format.
        - » There will be a toleration APAR for earlier releases so the they recognize a KDS is in the new format and fail gracefully.
      - When the web deliverable level is using a KDS in the old format it will not perform any of the new functions associated with this line item.
      - A new migration Health Check ICSFMIG77A1_TKDS will be created to check the TKDS to ensure it can be migrated to the format required for KDS Key Utilization function.

Crypto HCR77A1 Migration Considerations (5 of 5)

- **UDX (User Defined eXtension)**
  - Extends the functionality of IBM's CCA (Common Cryptographic Architecture) application program
    - Customized cryptographic verb controls per customer
  - UDX interfaces using hardware control blocks and ICSF control blocks
    - Therefore if hardware platform changes, or ICSF level changes, or both, then
      - UDX must updated for the new control blocks
        - » If a customer has UDX, they would already know this
  - **Starting with the Cryptographic Support for z/OS V1R13-z/OS V21R1 web deliverable some user defined extensions are shipped with the web deliverable.**

Deliverable Name	FMID	Applicable z/OS Releases	Avail	EoM
z/OS or z/OS.e V1.3 or V1.4	HCR7706	z/OS V1.3 and z/OS V1.4	3/2002	9/2004
z990 Cryptographic CP Assist Support for z/OS V1.3[1]	HCR7708	z/OS V1.3	6/2003	10/2003
z/OS V1.4 z990 Compatibility Support or z/OS.e z990 Coexistence	HCR7708	z/OS V1.4	6/2003	10/2003
z/OS V1.4 z990 Exploitation Support or z/OS.e Coexistence Update feature	HCR7708	z/OS V1.4	10/2003	12/2006
z990 Cryptographic Support [2]	HCR770A	OS/390 V2.10, z/OS 1.2, z/OS 1.3, z/OS V1.4, any z/OS V1.4 features, and z/OS V1.5	9/2003	5/2004
z/OS or z/OS.e V1.5	HCR7708	z/OS V1.5	3/2004	9/2004
z/OS or z/OS.e V1.6	HCR770A	z/OS V1.6	9/2004	10/2005
z990 and z890 Enhancements to Cryptographic Support [3]	HCR770B	OS/390 V2.10, z/OS V1.2, z/OS V1.3, z/OS V1.4 and z/OS V1.5	5/2004	TBD
ICSF 64-bit Virtual Support for Z/OS V1.6 and z/OS.e V1.6 [4]	HCR7720	z/OS V1.6	12/2004	9/2005
z/OS or z/OS.e V1.7	HCR7720	z/OS V1.7	9/2005	10/2006
Cryptographic Support for z/OS V1R6/R7 and z/OS.e V1R6/R7[5]	HCR7730	z/OS V1.6 and z/OS V1.7	9/2005	5/2006
Enhancements to Cryptographic Support for z/OS and z/OS.e V1R6/R7[6]	HCR7731	z/OS V1.6 and z/OS V1.7	5/2006	11/2007
z/OS or z/OS.e V1.8	HCR7731	z/OS V1.8	9/2006	10/2007
z/OS V1.9	HCR7740	z/OS V1.9	9/2007	10/2008
Cryptographic Support for z/OS V1R7-V1R9 and z/OS.e V1R7-V1R8 web deliverable[7]	HCR7750	z/OS V1.7, z/OS V1.8 and z/OS V1.9	9/2007	10/2011
z/OS V1.10	HCR7750	z/OS V1.10	9/2008	10/2009
Cryptographic Support for z/OS V1.8 through z/OS V1.10 and z/OS.e V1.8 web deliverable[8]	HCR7751	z/OS V1.7, z/OS V1.8, z/OS V1.9, z/OS V1.10	11/2008	11/2009
z/OS V1.11	HCR7751	z/OS V1.11	9/2009	10/2010
Cryptographic Support for z/OS V1R9-V1R11 Web deliverable[9]	HCR7770	z/OS V1.9, z/OS V1.10, z/OS V1.11	11/2009	9/2010
z/OS V1.12	HCR7770	z/OS V1.12	9/2010	10/2011
Cryptographic Support for z/OS V1R10-V1R12 Web deliverable[10]	HCR7780	z/OS V1.10, z/OS V1.11, z/OS V1.12	9/2010	TBD
z/OS V1.13	HCR7780	z/OS V1.13	9/2011	1/2014
Cryptographic Support for z/OS V1R11-V1R13 Web deliverable[11]	HCR7790	z/OS V1.11, z/OS V1.12, z/OS V1.13	9/2011	TBD
Cryptographic Support for z/OS V1R12-V1R13 Web deliverable[12]	HCR77A0	z/OS V1.12, z/OS V1.13	9/2012	TBD
z/OS V2.1	HCR77A0	z/OS V2.1	9/2013	1Q2016*
Cryptographic Support for z/OS V1R13-z/OS V21R1 Web deliverable[13]	HCR77A1	z/OS V1.13, z/OS V2.1	9/2013	TBD
Enhanced Cryptographic Support for z/OS V1R13-z/OS V21R1 Web deliverable[14]	HCR77B0	z/OS V1.13, z/OS V2.1	3/2015	TBD
z/OS V2.2*	HCR77B0	z/OS V2.2	9/2015*	2H2017*

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

zEnd

The future runs on z Systems