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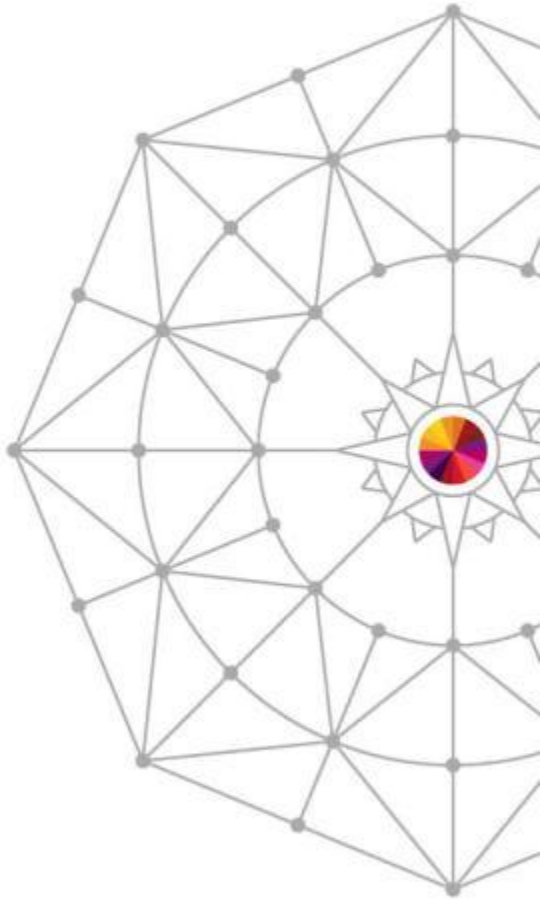
SHARE

Migrating To zEC12 : A Journey In Performance

Meral Temel
İşbank

12 March 2014
14995



SHARE in Anaheim

Migrating To zEC12:
A Journey In Performance

Agenda

- Who is İşBank ?
- Mainframe Configuration
- Z10 – zEC12 Configuration Differences
- Migration Process (Steps & Hints & Tips)
- zPCR Study
- Z10 To zEC12 Upgrade Performance Analiz Using SMF113 Counters
- CPU - DASD I/O – CF - Memory View
- Checking Side Effects
- Planned Features
- References
- More Information – Backup Slides

Who Is İŞBANK ?

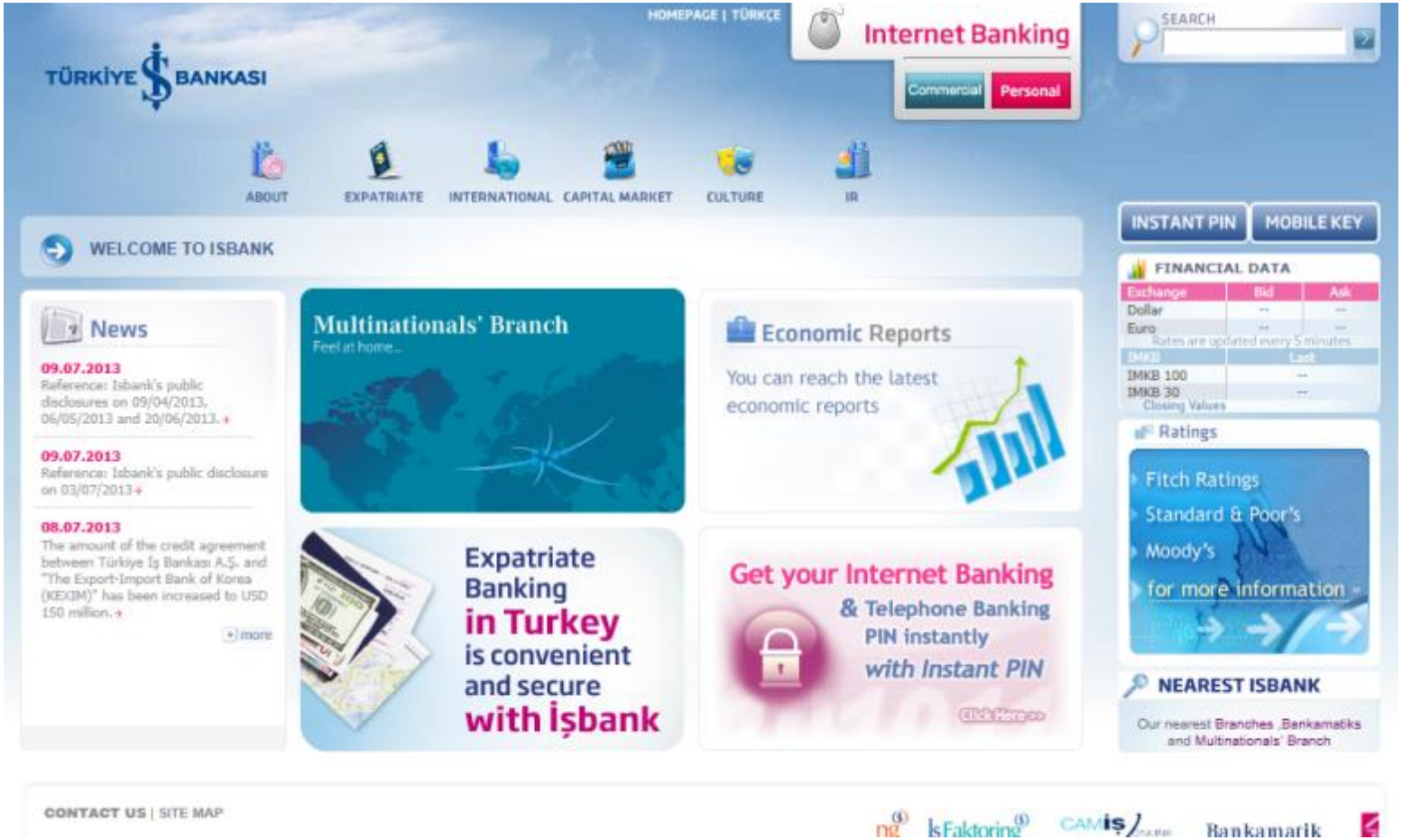
- The Biggest Bank Of Turkey
- 5521 ATMs
- 1296 Branches In Turkey, 20 Branches Outside Turkey
- Has The Highest Profit According To All Bank Announcements 2013
- Member Of SHARE Inc.

Who Is İŞBANK ?

BRANCHES

Who Is İŞBANK ?

INTERNET BANKING



Who Is İŞBANK ?

ATM

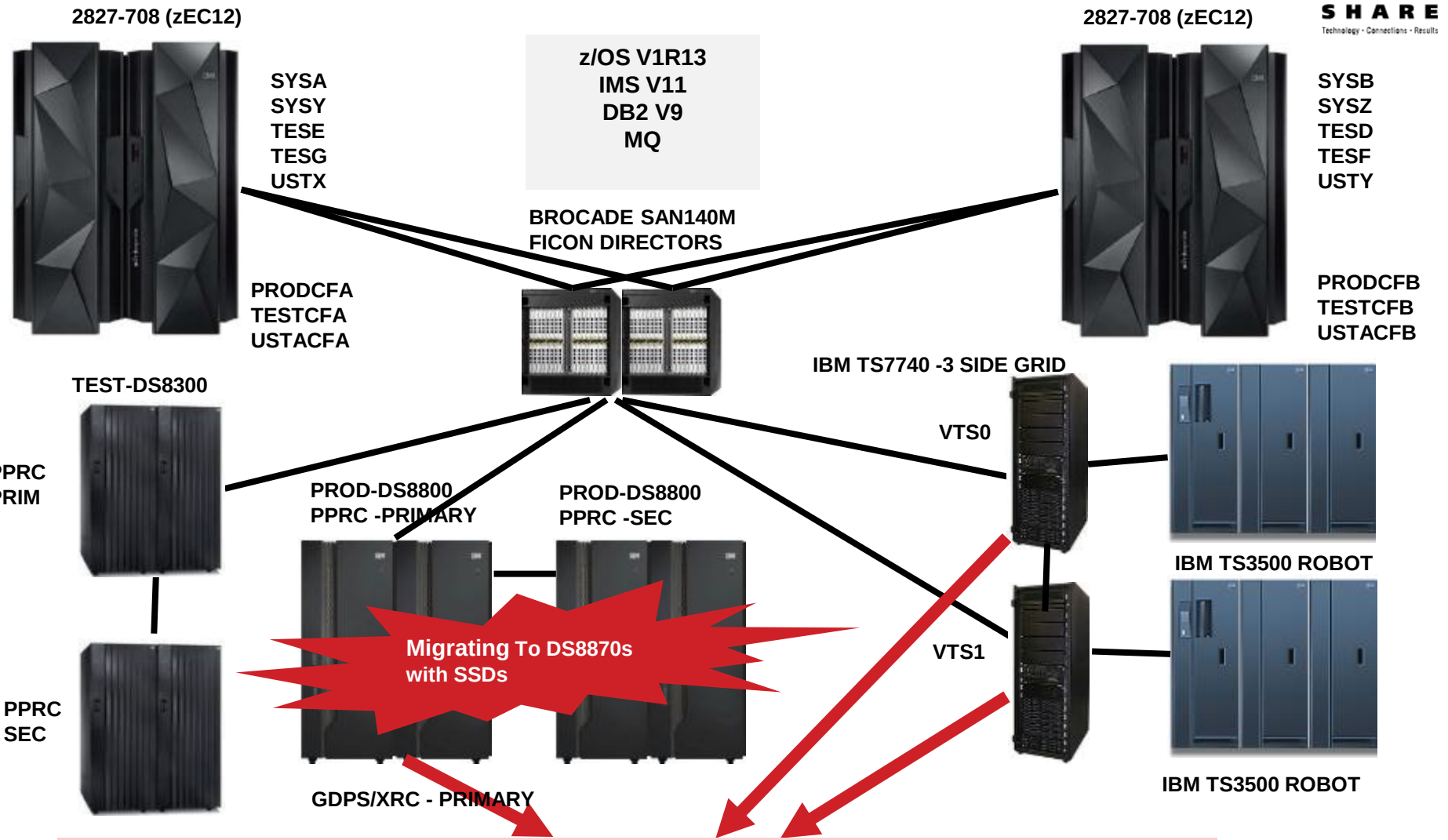
İŞCEP
Mobile Phone Application

İŞBANK IPAD FINANCE CENTER
Application

Who Is İŞBANK ?

Credit Cards

İşbank – Mainframe Configuration



İşbank – zEC12 Configuration Details

2827-708 (zEC12)

8 GCP (5.5 GHz)
3 ICF,3 zIIP,1 IFL
10063 IBM PCI
10062,8 MIPS(Average RNI)
1224 MSU
1257,9 MIPS/CP
153 MSU/CP
64777 SU/sec
192 GB Memory
- 160 GB Customer
- 32 GB HSA
18 FICONExpress 8S
(32port- 32 FICON Channel)
10 HCA3-Fanout Cards
20 Infiniband3 CF Link
12 OSA-Express4S 10 GbE
SR 1 port
4 OSA-Express4S 1000BASE-T
4 Crypto Express4S
2 FlashExpress
zAware

2827-708 (zEC12)

8 GCP (5.5 GHz)
3 ICF,3 zIIP
10063 IBM PCI
10062,8 MIPS(Average RNI)
1224 MSU
1257,9 MIPS/CP
153 MSU/CP
64777 SU/sec
192 GB Memory
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18 FICONExpress 8S
(32port- 32 FICON Channel)
10 HCA3-Fanout Cards
20 Infiniband3 CF Link
12 OSA-Express4S
10 GbE SR 1 port
4 OSA-Express4S 1000BASE-T
4 Crypto Express4S

Migration Steps

DATE	STEP
03.May.13	SYSY z/OS V1R13 Upgrade
18.May.13	SYSZ z/OS V1R13 Upgrade
25/26-May 2013	SYSA/SYSB z/OS V1R13 Upgrade
7-June-2013	DB2 RSU
8-June-2013	PRODCF2 zEC12 + SYSY zEC12 Upgrade
23-June-2013	PRODCF1 zEC12 + SYSZ zEC12 Upgrade
7-July-2013	SYSA/SYSB/GKP1 zEC12 Upgrade + IMS IRLM new CF + IMS QSAM new CF

- z/OS v1R11 To V1R13 Upgrade
- Software /Hardware Products Maintenance Level Check- Upgrades
- Hardware Connectivity – FICONs,OSA-CC Console Network, OSA 10Gb IP Network Connections
- OSA-CC Console Definitions
- Time Checking For both zEC12 SEs.
- Adding zEC12s to STP Network
- GDPS BCPII API Definitions On zEC12 SEs
- Usta LPARS/CFs To zEC12
- Test LPARS/CFs To zEC12
- PRODCFB + SYSY LPAR To zEC12
- PRODCFA + SYSZ LPAR To zEC12
- SYSA & SYSB To zEC12

Migration Process - Hints

- Use CFSizer Tool To Estimate Structure Sizes
  - Not good for some structures
  - Double-check Power Of 2 for Lock Structure
- Use Resourcelink website to check your missing MCLs
  - Apply all of them before go into Production
  - Several for zAWARE , one about Hyperdispatch, one important about zFlash
- After using CHPID Mapping Tool, check your CHPID numbers
  - You need to rearrange if you have rule like ‘‘odd numbers for one FICON Director and even numbers for other FICON Director’’. CHPID Mapping Tool Does not care about these. Better is run tool then do cabling. Not the other way.
- ICB4 to Infiniband ; Although it is said as 1-1 ,use more than one for each, we did 2ICB4 :3 Infiniband Physical connection.
- Be careful about z10 Infiniband Earlier Protocol Support- Not IFB3.

  IF CF is earlier than LPAR, let loved structures stay in old CF in order not to use Infiniband instead of IC. IC is still the best.
- If you have lack of subchannel , you must use more than 1:1 anyway.
- Although it is NOW acceptable ,prefer to use one CHPID per port for Production.
- Know your workload before, so that you can have idea where your bottleneck is.

Sample RMF Overview Report That I Used In This Study

```
//SMT1RMFP JOB  CLASS=A,NOTIFY=&SYSUID,MSGCLASS=X,SCHENV=SYSSYSZ,
//  USER=IS93081,PASSWORD=
//STEP1    EXEC PGM=IFASMFDP,REGION=32M
//DUMPIN   DD  DSN=ISB.SMFBACK.SYSA.Y2013.A07.G15,DISP=SHR
//DUMPOUT  DD  DSN=&&PAS,DISP=(,PASS),UNIT=SYSDA,
//         SPACE=(CYL,(500,100)),DCB=(LRECL=137,RECFM=VBA,BLKSIZE=1693)
//SYSPRINT DD  SYSOUT=X
//SYSIN    DD  *
 INDD(DUMPIN,OPTIONS(DUMP))
 OUTDD(DUMPOUT,TYPE(74))
 START(0900)
 END(1700)
//STEP2    EXEC PGM=SORT
//SORTIN   DD  DSN=&&PAS,DISP=(OLD,DELETE)
//SYSOUT   DD  SYSOUT=X
//SORTOUT  DD DSN=&&PASA,DISP=(,PASS),
//         SPACE=(CYL,(500,100))
//SORTWK01 DD  SPACE=(CYL,2)
//SORTWK02 DD  SPACE=(CYL,2)
//SORTWK03 DD  SPACE=(CYL,2)
//EXITLIB  DD  DSN=SYS1.LINKLIB,DISP=SHR
//SYSIN    DD  *
    SORT FIELDS=(11,4,CH,A,7,4,CH,A),EQUALS
    MODS E15=(ERBPPE15,36000,,N),E35=(ERBPPE35,3000,,N)
//*  PRODUCE SUMMARY REPORT
//*
//STEP5    EXEC PGM=ERBRMFPP,REGION=32M
//MFPINPUT DD  DSN=&&PASA,DISP=(OLD,DELETE)
//MFPMSGDS DD  SYSOUT=X
//PPRPTS   DD  SYSOUT=X
//SYSRPTS  DD  SYSOUT=X
//SYSIN     DD  *
 ETOD(0900,1700)
 STOD(0900,1700)
 RTOD(0900,1700)
 SYSOUT(A)
 OVERVIEW(REPORT)
 SUMMARY(INT,TOT)
 OVW(IMSLSST(SYNCST(IMSP_IRLM)))
 OVW(IMSLAST(ASYNCST(IMSP_IRLM)))
 OVW(IMSLSRT(SYNCRT(IMSP_IRLM)))
 OVW(IMSLART(ASYNCRT(IMSP_IRLM)))
```

Effect of Migration From z10s To zEC12
CPU VIEW

Differences Between z10s & zEC12s In Our Configuration (CPU VIEW)

2097-714 (z10)

2097-710 (z10)

2827-708 (zEC12)

2827-708 (zEC12)

TOTAL MIPS 16460	22% Increase	TOTAL MIPS 20126
TOTAL SW MSU 2014	22% Increase	TOTAL SW MSU 2448
MIPS/CP 668 - 710	77-88% Increase	MIPS/CP 1258
SW MSU/CP 81.3- 87.5	75-88% Increase	SW MSU/CP 153
SU/Sec 33613-36281	79-93% Increase	SU/Sec 64777
ITR- Avg RNI 12.69 – 16.71	%7.6-%41.6 Increase	ITR-Avg RNI 17.98

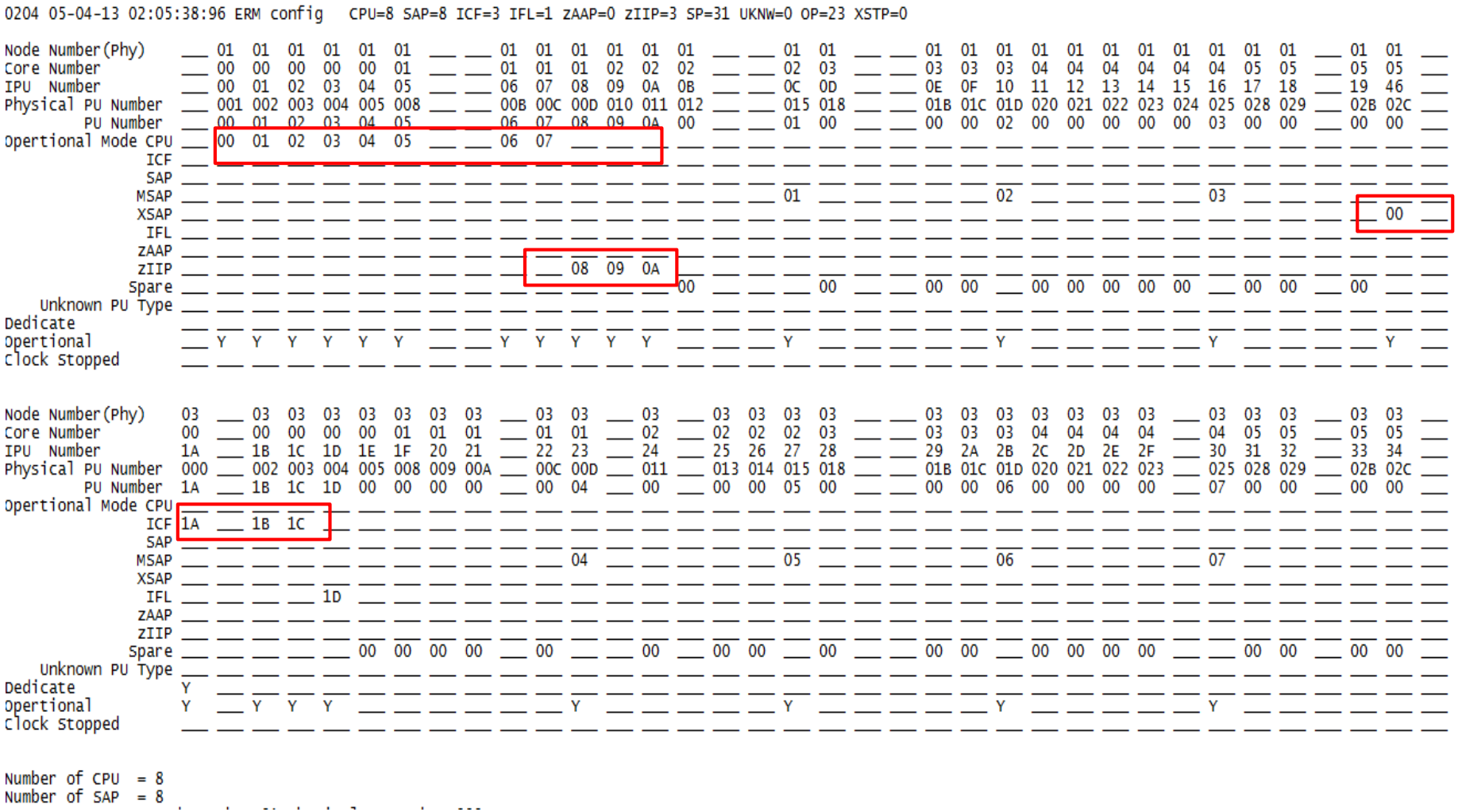
Model	# of CPs	IBM PCI	Avg RNI MIPS	Avg RNI MIPS/	MP	Low RNI MIPS	Low-Avg RNI MIPS	Avg-Hi RNI MIPS	High RNI MIPS	SU/Sec	UP SU/Sec	Common Name	Proc Grp	S/W MSUs	MIPS/ S/W	H/W MSUs
2827-708	8	10063	10062,8	1257,9	0,83	11076,5	10545,3	9487,3	8974,0	64777,3279	78048,7805	zEC12	IMLC	1224	8,2	1866
2097-714	14	9355	9354,6	668,2	0,74	10882,5	10060,9	8659,8	8061,0	33613,4454	47619,0476	z10-EC	IMLC	1139	8,2	1694
2097-710	10	7105	7105,2	710,5	0,79	8076,7	7559,8	6610,6	6180,4	36281,1791	47619,0476	z10-EC	IMLC	875	8,1	1306

z10s & zEC12s Differences- Memory

2097-714 (z10)	2097-710 (z10)	2827-708 (zEC12)	2827-708 (zEC12)
			
TOTAL 96 GB 80 GB Customer 16 GB HSA	TOTAL 96 GB 80 GB Customer 16 GB HSA	TOTAL 192GB 160GB Customer 32 GB HSA	TOTAL 192GB 160GB Customer 32 GB HSA
SYSA: 27 GB SYSY: 16 GB PRODCF1: 14 GB	SYSB: 20 GB SYSZ: 16 GB PRODCF2: 12 GB	SYSA: 40 GB +8 Reserve SYSY: 20 GB + 4 PRODCF1: 24 GB	SYSB: 40 GB + 8 Reserve SYSZ: 20 GB + 4 PRODCF2: 24 GB

*** We increased Production and Test Syplex Images' Memory More.

Where Are My CPs, ICFs, zIIPs, IFL?



```
0204 05-04-13 02:05:38:96 ERM config   CPU=8 SAP=8 ICF=3 IFL=1 zAAP=0 zIIP=3 SP=31 UKNW=0 OP=23 XSTP=0

Node Number(Phy)    ___ 01 01 01 01 01 01 ___ ___ 01 01 01 01 01 01 ___ ___ 01 01 ___ ___ 01 01 01 01 01 01 01 01 01 01 ___ 01 01 ___
Core Number         ___ 00 00 00 00 00 01 ___ ___ 01 01 01 02 02 02 ___ ___ 02 03 ___ ___ 03 03 03 04 04 04 04 04 04 05 05 ___ 05 05 ___
IPU  Number         ___ 00 01 02 03 04 05 ___ ___ 06 07 08 09 0A 0B ___ ___ 0C 0D ___ ___ 0E 0F 10 11 12 13 14 15 16 17 18 ___ 19 46 ___
Physical PU Number  ___ 001 002 003 004 005 008 ___ ___ 00B 00C 00D 010 011 012 ___ ___ 015 018 ___ ___ 01B 01C 01D 020 021 022 023 024 025 028 029 ___ 02B 02C ___
        PU Number   ___ 00 01 02 03 04 05 ___ ___ 06 07 08 09 0A 00 ___ ___ 01 00 ___ ___ 00 00 02 00 00 00 00 00 03 00 00 ___ 00 00 ___
Opertional Mode CPU ___ 00 01 02 03 04 05 ___ ___ 06 07 ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              ICF   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              SAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             MSAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 01 ___ ___ ___ ___ 02 ___ ___ ___ ___ ___ 03 ___ ___ ___ ___
             XSAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 00 ___
              IFL   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zAAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zIIP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 08 09 0A ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
            Spare   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 00 ___ ___ ___ 00 ___ ___ 00 00 ___ 00 00 00 00 00 ___ 00 00 ___ 00 ___ ___
    Unknown PU Type ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Dedicate            ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Opertional          ___ Y Y Y Y Y Y ___ ___ Y Y Y Y Y ___ ___ ___ Y ___ ___ ___ ___ ___ Y ___ ___ ___ ___ ___ Y ___ ___ ___ ___ Y ___
Clock Stopped       ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___


Node Number(Phy)    03 ___ 03 03 03 03 03 03 03 ___ 03 03 ___ 03 ___ 03 03 03 03 ___ ___ 03 03 03 03 03 03 03 ___ 03 03 03 ___ 03 03 ___
Core Number         00 ___ 00 00 00 00 01 01 01 ___ 01 01 ___ 02 ___ 02 02 02 03 ___ ___ 03 03 03 04 04 04 04 ___ 04 05 05 ___ 05 05 ___
IPU  Number         1A ___ 1B 1C 1D 1E 1F 20 21 ___ 22 23 ___ 24 ___ 25 26 27 28 ___ ___ 29 2A 2B 2C 2D 2E 2F ___ 30 31 32 ___ 33 34 ___
Physical PU Number  000 ___ 002 003 004 005 008 009 00A ___ 00C 00D ___ 011 ___ 013 014 015 018 ___ ___ 01B 01C 01D 020 021 022 023 ___ 025 028 029 ___ 02B 02C ___
        PU Number   1A ___ 1B 1C 1D 00 00 00 00 ___ 00 04 ___ 00 ___ 00 00 05 00 ___ ___ 00 00 06 00 00 00 00 ___ 07 00 00 ___ 00 00 ___
Opertional Mode CPU ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              ICF   1A ___ 1B 1C ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              SAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
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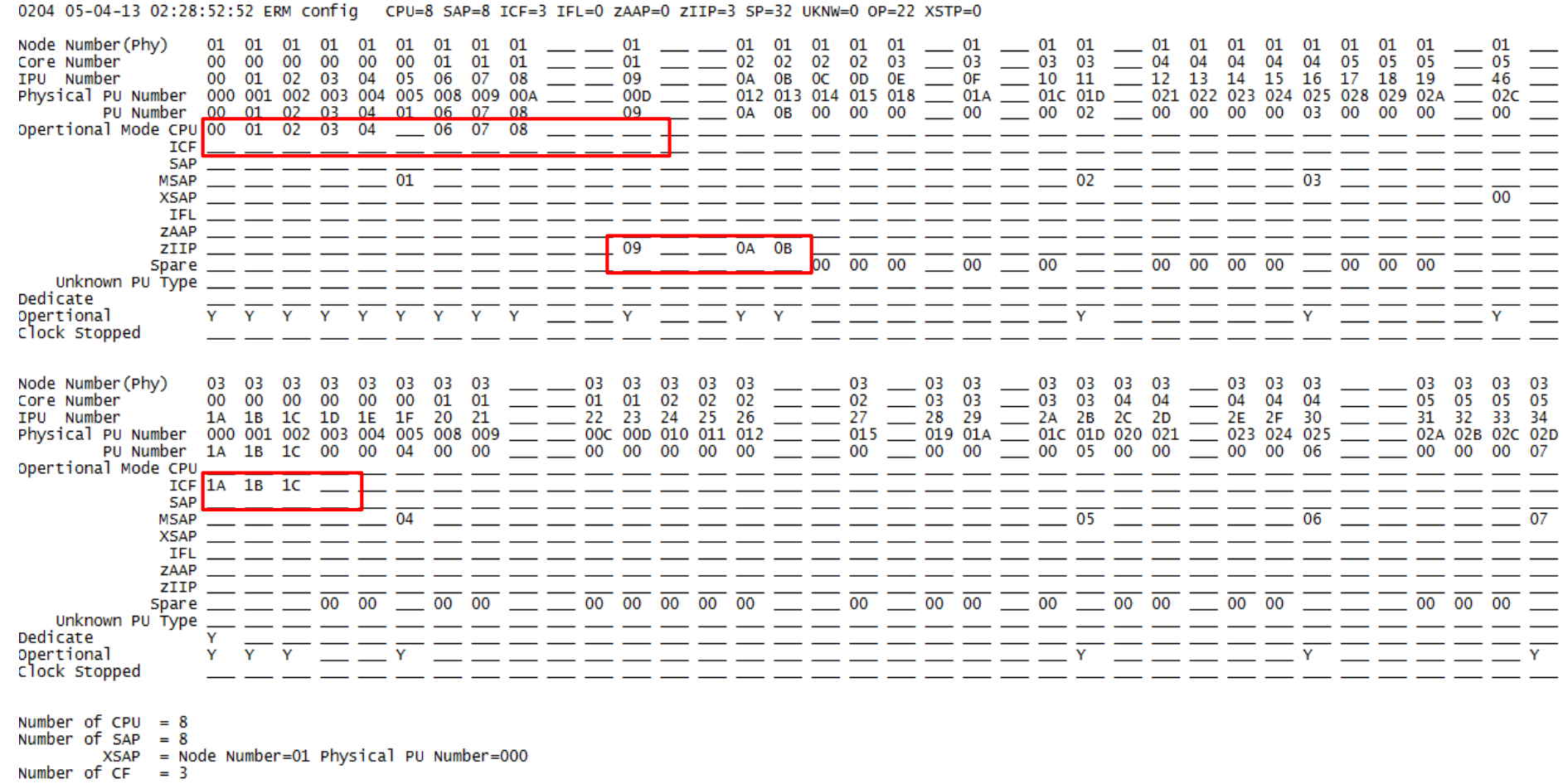
             XSAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              IFL   ___ ___ ___ ___ 1D ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zAAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zIIP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
            Spare   ___ ___ ___ ___ ___ 00 00 00 00 ___ 00 ___ ___ 00 ___ 00 00 ___ 00 ___ ___ 00 00 ___ 00 00 00 00 ___ ___ 00 00 ___ 00 00 ___
    Unknown PU Type ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Dedicate            Y ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Opertional          Y ___ Y Y Y ___ ___ ___ ___ ___ ___ Y ___ ___ ___ ___ ___ Y ___ ___ ___ ___ ___ Y ___ ___ ___ ___ ___ Y ___ ___ ___ ___ ___ ___
Clock Stopped       ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___


Number of CPU  = 8
Number of SAP  = 8
```

Where Are My CPs,ICFs,zIIPs ?



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Core Number         00  00  00  00  00  00  01  01  01  ___ ___ 01  ___ ___ 02  02  02  02  03  ___ 03  ___ 03  03  ___ 04  04  04  04  04  05  05  05  ___ 05  ___
IPU  Number         00  01  02  03  04  05  06  07  08  ___ ___ 09  ___ ___ 0A  0B  0C  0D  0E  ___ 0F  ___ 10  11  ___ 12  13  14  15  16  17  18  19  ___ 46  ___
Physical PU Number  000 001 002 003 004 005 008 009 00A ___ ___ 00D ___ ___ 012 013 014 015 018 ___ 01A ___ 01C 01D ___ 021 022 023 024 025 028 029 02A ___ 02C ___
        PU Number   00  01  02  03  04  01  06  07  08      ___ 09  ___ ___ 0A  0B  00  00  00  ___ 00  ___ 00  02  ___ 00  00  00  00  03  00  00  00  ___ 00  ___
Opertional Mode CPU 00  01  02  03  04  ___ 06  07  08  ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              ICF   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              SAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             MSAP   ___ ___ ___ ___ ___ 01  ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 02  ___ ___ ___ ___ ___ 03  ___ ___ ___ ___ ___ ___
             XSAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 00  ___ ___
              IFL   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zAAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zIIP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 09  ___ ___ 0A  0B  ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
            Spare   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 00  00  00  ___ 00  ___ 00  ___ ___ 00  00  00  00  ___ 00  00  00  ___ ___ ___ ___
    Unknown PU Type ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Dedicate            ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Opertional          Y   Y   Y   Y   Y   Y   Y   Y   Y   ___ ___ Y   ___ ___ Y   Y   ___ ___ ___ ___ ___ ___ Y   ___ ___ ___ ___ ___ Y   ___ ___ ___ ___ Y   ___ ___
Clock Stopped       ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___


Node Number(Phy)    03  03  03  03  03  03  03  03  ___ ___ 03  03  03  03  03  ___ ___ 03  ___ 03  03  ___ 03  03  03  03  ___ 03  03  03  ___ ___ 03  03  03  03
Core Number         00  00  00  00  00  00  01  01  ___ ___ 01  01  02  02  02  ___ ___ 02  ___ 03  03  ___ 03  03  04  04  ___ 04  04  04  ___ ___ 05  05  05  05
IPU  Number         1A  1B  1C  1D  1E  1F  20  21  ___ ___ 22  23  24  25  26  ___ ___ 27  ___ 28  29  ___ 2A  2B  2C  2D  ___ 2E  2F  30  ___ ___ 31  32  33  34
Physical PU Number  000 001 002 003 004 005 008 009 ___ ___ 00C 00D 010 011 012 ___ ___ 015 ___ 019 01A ___ 01C 01D 020 021 ___ 023 024 025 ___ ___ 02A 02B 02C 02D
        PU Number   1A  1B  1C  00  00  04  00  00  ___ ___ 00  00  00  00  00  ___ ___ 00  ___ 00  00  ___ 00  05  00  00  ___ 00  00  06  ___ ___ 00  00  00  07
Opertional Mode CPU ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              ICF   1A  1B  1C  ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              SAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             MSAP   ___ ___ ___ ___ ___ 04  ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ 05  ___ ___ ___ ___ ___ 06  ___ ___ ___ ___ ___ 07
             XSAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
              IFL   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zAAP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
             zIIP   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
            Spare   ___ ___ ___ 00  00  ___ 00  00  ___ ___ 00  00  00  00  00  ___ ___ 00  ___ 00  00  ___ 00  ___ 00  00  ___ 00  00  ___ ___ ___ 00  00  00  ___
    Unknown PU Type ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Dedicate            Y   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___
Opertional          Y   Y   Y   ___ ___ Y   ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ Y   ___ ___ ___ ___ ___ Y   ___ ___ ___ ___ ___ Y
Clock Stopped       ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___ ___


Number of CPU  = 8
Number of SAP  = 8
      XSAP  = Node Number=01 Physical PU Number=000
Number of CF   = 3
```

LPAR Configuration Design – IBM WLM Website

ISB01 BEFORE UPGRADE **Prod1 : SYSA Prod3: SYSZ Test1: TESF Test3:TESG**

LPARDesign-HD-V4-T00 LPAR DEFINITION (CP) TOLERATION%=0

		ψMachine	Shared-Pool
CFG-LP-VALID?	NO	#PhyProc	14	14
Machine-type	2097-714	#LPs (non-ICF, non-DED)	46	
MSU	1139	Ratio LP/PP (base)	3,29	
Total Weight	1374	LSPR-AVG-V1R13-MI	9355	

1 - CONFIG. VALIDATION | 2 - HIPERDISPATCH | PRINT | 3 - GoTo ZXXP | Go To EXPERT

LPARNAME	WEIGHT	#LP	%SHARE(by pool)	"MIPS"	Guaranteed#PP	NON-HD Share%/LP	MinReq#LP	Check#LP	HD-HIGH#	HD-MED#	HD-MED%	HD-LOW#	#Active LPs	#Report LPs
Prodg1	60	7	4%	409	0,57	8%	1	OK	0	1	57,0%	6	2	1
Prod1	900	14	66%	6128	9,02	64%	10	OK	8	2	51,2%	4	10	10
Prod3	400	14	29%	2723	4,27	31%	5	OK	3	2	63,7%	9	5	5
Testg1	3	2	0%	20	0,03	1%	1	OK	0	1	2,8%	1	2	1
Test1	5	4	0%	34	0,05	1%	1	OK	0	1	4,7%	3	2	1
Test3	5	4	0%	34	0,05	1%	1	OK	0	1	4,7%	3	2	1
Usta	1	1	0%	7	0,01	1%	1	OK	0	1	0,9%	0	1	1

ISBANK01 AFTER UPGRADE **Prod1 : SYSA Prod3: SYSZ Test1: TESE Test3:TESG**

LPARDesign-HD-V4-T00 LPAR DEFINITION (CP) TOLERATION%=0

		ψMachine	Shared-Pool
CFG-LP-VALID?	NO	#PhyProc	8	8
Machine-type	2827-708	#LPs (non-ICF, non-DED)	33	
MSU	1224	Ratio LP/PP (base)	4,13	
Total Weight	1000	LSPR-AVG-V1R13-MI	10063	

1 - CONFIG. VALIDATION | 2 - HIPERDISPATCH | PRINT | 3 - GoTo ZXXP | Go To EXPERT

LPARNAME	WEIGHT	#LP	%SHARE(by pool)	"MIPS"	Guaranteed#PP	NON-HD Share%/LP	MinReq#LP	Check#LP	HD-HIGH#	HD-MED#	HD-MED%	HD-LOW#	#Active LPs	#Report LPs
Prodg1	40	7	4%	403	0,32	5%	1	OK	0	1	32,0%	6	2	1
Prod1	580	8	58%	5837	4,64	58%	5	OK	4	1	64,0%	3	5	5
Prod3	320	8	32%	3220	2,56	32%	3	OK	2	1	56,0%	5	3	3
Testg1	2	2	0%	20	0,02	1%	1	OK	0	1	1,6%	1	2	1
Test1	55	3	6%	553	0,44	15%	1	OK	0	1	44,0%	2	2	1
Test3	2	4	0%	20	0,02	0%	1	OK	0	1	1,6%	3	2	1
Usta	1	1	0%	10	0,01	1%	1	OK	0	1	0,8%	0	1	1

Norman Hollander – IBM Has Also One version
Send email if you want it and give it a try….

LPAR Configuration Design – IBM WLM Website

ISB02 BEFORE UPGRADE **Prod2 : SYSB Prod3: SYSZ Test2:TESD Test4:TESE**

LPARDesign-HD-V4-T00 LPAR DEFINITION (CP) TOLERATION%=0

		ψMachine	Shared-Pool
CFG-LP-VALID?	NO	#PhyProc	10	10
Machine-type	2097-710	#LPs (non-ICF, non-DED)	38	
MSU	875	Ratio LP/PP (base)	3,80	
Total Weight	1000	LSPR-AVG-V1R13-MI	7105	

1 - CONFIG. VALIDATION | 2 - HIPERDISPATCH | PRINT | 3 - GoTo ZXXP | Go To EXPERT

LPARNAME	WEIGHT	#LP	%SHARE(by pool)	"MIPS"	Guaranteed#PP	NON-HD Share%/LP	MinReq#LP	Check#LP	HD-HIGH#	HD-MED#	HD-MED%	HD-LOW#	#Active LPs	#Report LPs
Prodg2	1	10	0%	7	0,01	0%	1	OK	0	1	1,0%	9	2	1
Prod2	390	10	39%	2771	3,90	39%	4	OK	3	1	90,0%	6	4	4
Prod4	380	10	38%	2700	3,80	38%	4	OK	3	1	80,0%	6	4	4
test2	110	3	11%	782	1,10	37%	2	OK	0	2	55,0%	1	2	2
test4	110	2	11%	782	1,10	55%	2	OK	0	2	55,0%	0	2	2
Ustag	1	2	0%	7	0,01	1%	1	OK	0	1	1,0%	1	2	1
Usta2	8	1	1%	57	0,08	8%	1	OK	0	1	8,0%	0	1	1

ISBANK02 AFTER UPGRADE **Prod2 : SYSB Prod3: SYSZ Test2:TESD Test4:TESE**

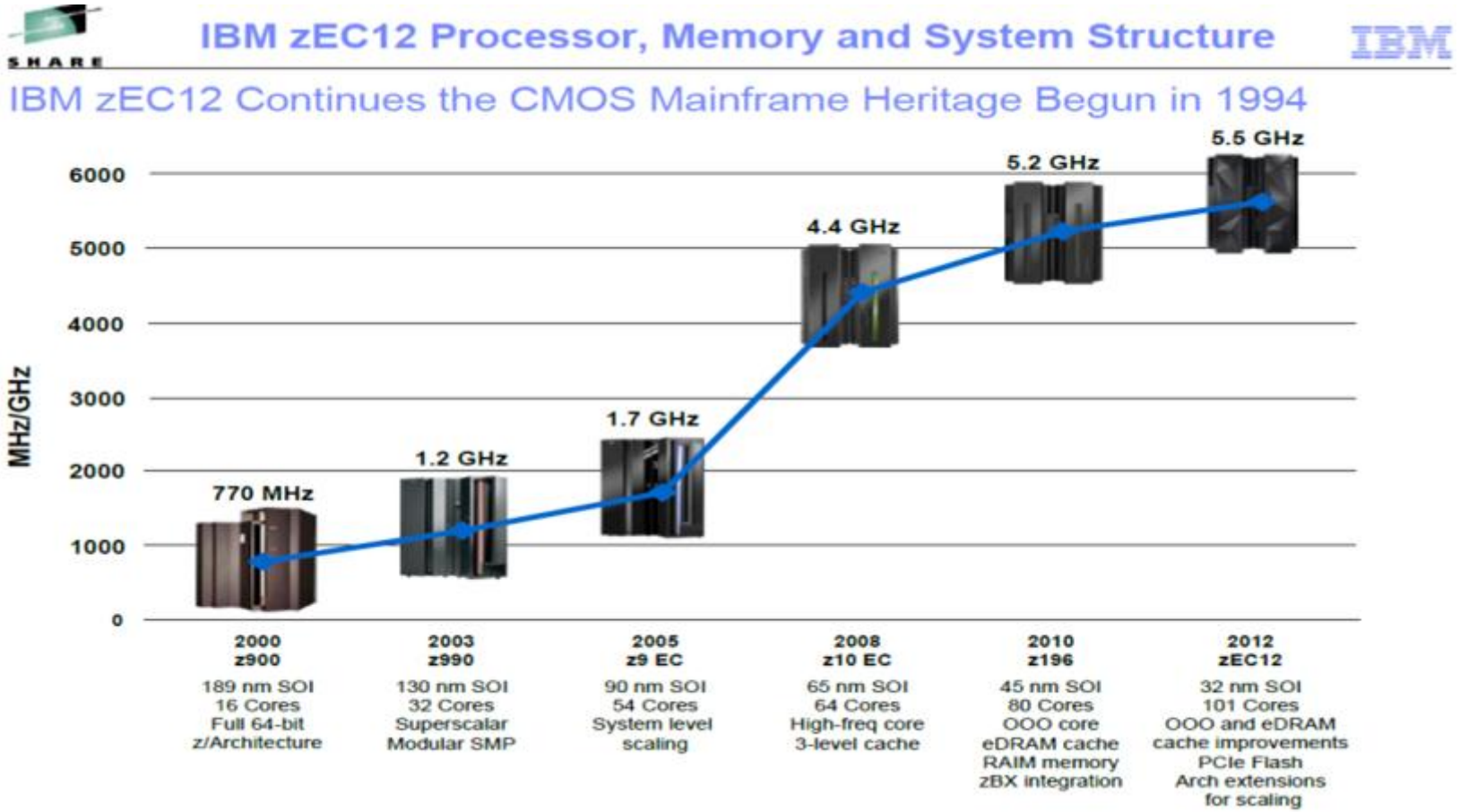
LPARDesign-HD-V4-T00 LPAR DEFINITION (CP) TOLERATION%=0

		ψMachine	Shared-Pool
CFG-LP-VALID?	NO	#PhyProc	8	8
Machine-type	2827-708	#LPs (non-ICF, non-DED)	32	
MSU	1224	Ratio LP/PP (base)	4,00	
Total Weight	1000	LSPR-AVG-V1R13-MI	10063	

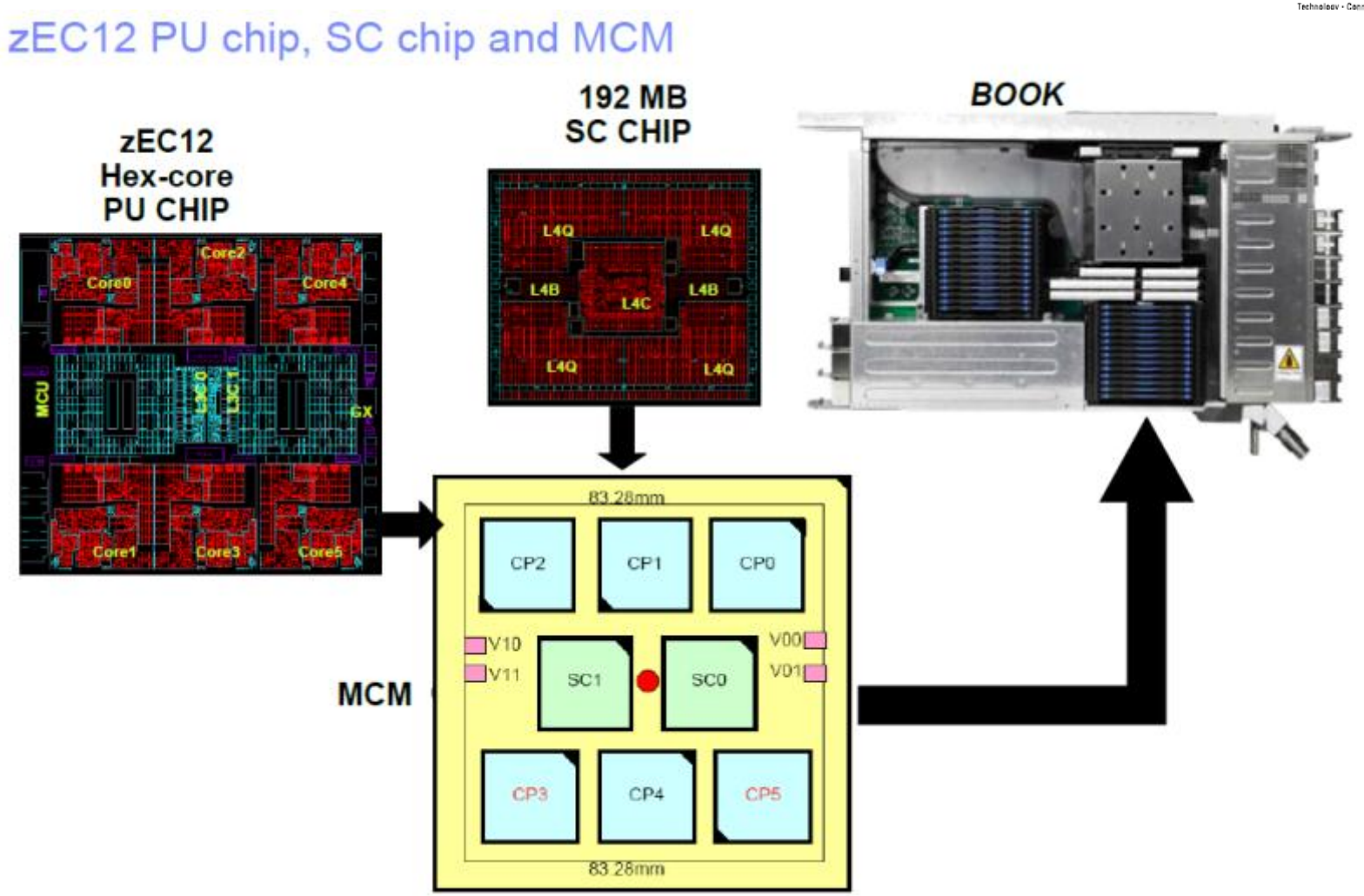
1 - CONFIG. VALIDATION | 2 - HIPERDISPATCH | PRINT | 3 - GoTo ZXXP | Go To EXPERT

LPARNAME	WEIGHT	#LP	%SHARE(by pool)	"MIPS"	Guaranteed#PP	NON-HD Share%/LP	MinReq#LP	Check#LP	HD-HIGH#	HD-MED#	HD-MED%	HD-LOW#	#Active LPs	#Report LPs
Prodg2	1	8	0%	10	0,01	0%	1	OK	0	1	0,8%	7	2	1
Prod2	580	8	58%	5837	4,64	58%	5	OK	4	1	64,0%	3	5	5
Prod4	320	8	32%	3220	2,56	32%	3	OK	2	1	56,0%	5	3	3
test2	85	4	9%	855	0,68	17%	1	OK	0	1	68,0%	3	2	1
test4	5	2	1%	50	0,04	2%	1	OK	0	1	4,0%	1	2	1
Ustag	1	1	0%	10	0,01	1%	1	OK	0	1	0,8%	0	1	1
Usta2	8	1	1%	81	0,06	6%	1	OK	0	1	6,4%	0	1	1

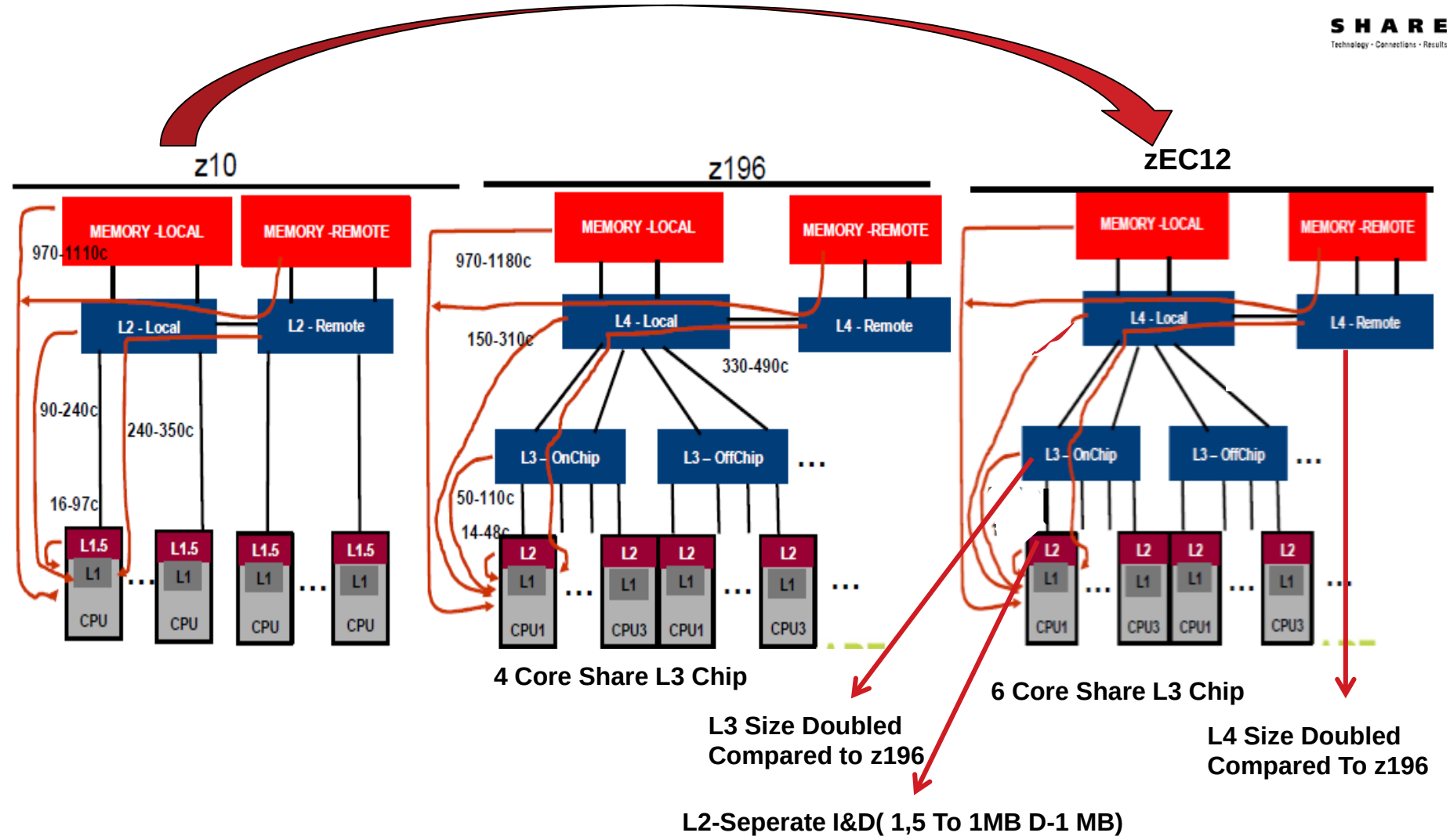
z10 – zEC12 Differences



z10 – zEC12 Differences

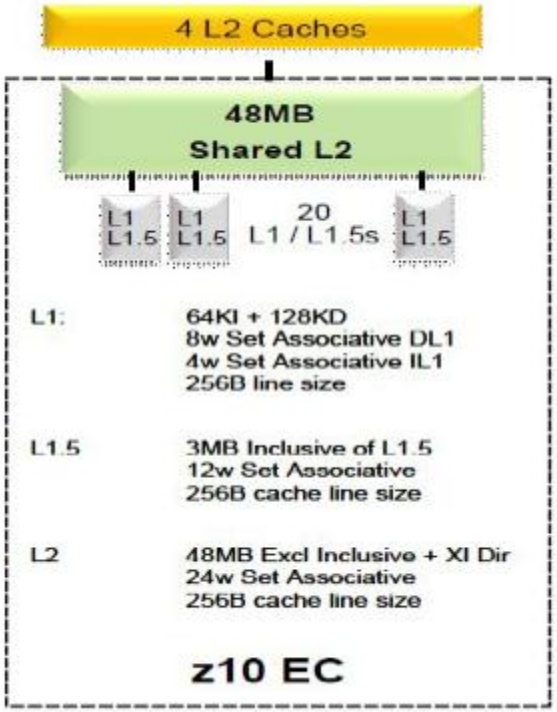


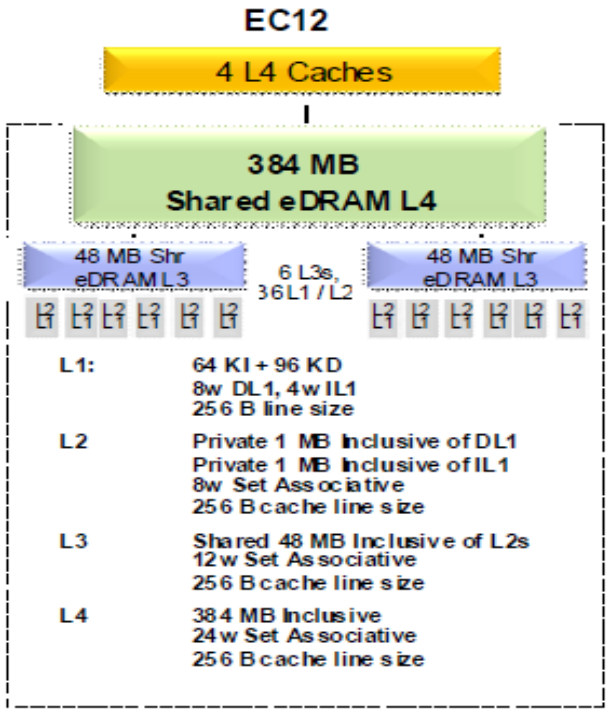
z10 – zEC12 Differences



z10 – zEC12 Differences

CacheLEVEL	z10	zEC12
L1 Cache	64KB D-128KB I	64KB D-96KB I
L1,5 Cache	3MB	N/A
L2 Cache	48MB	1MB D- 1MB-I
L3 Cache	N/A	48MB
L4 Cache	N/A	384MB





Workload Performance Is Sensitive To ….

Instruction Path Length For A Transaction Or Job

Instruction Complexity(Microprocessor Design)

Memory Hierarchy Or Nest

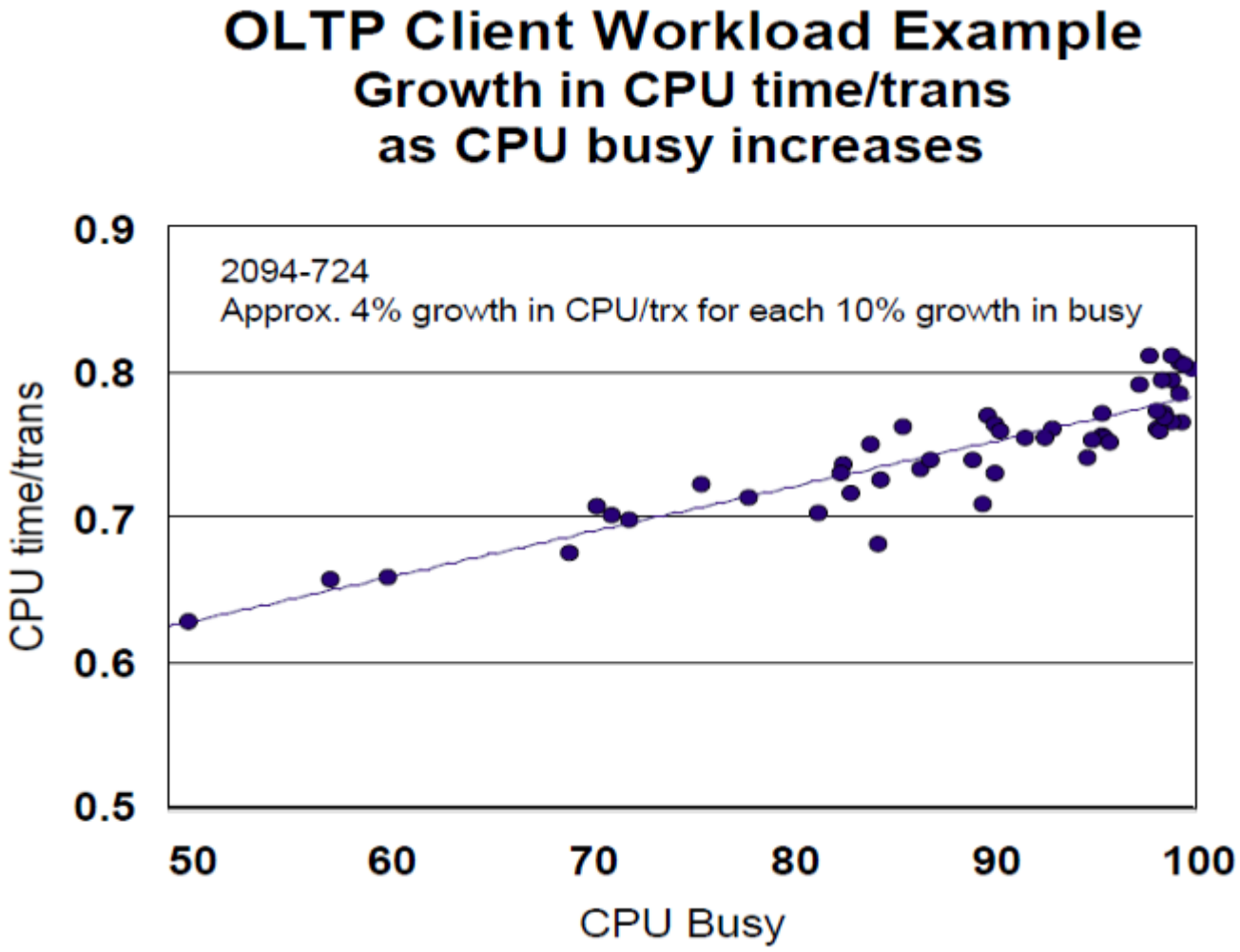
RNI – Relative Nest Intensity

DASD IO rate has been used for many years to separate workloads into two categories: those whose DASD IO per MSU (adjusted) is <30 (or DASD IO per PCI <5) and those higher than these values. The majority of production workloads fell into the "low IO" category and a LoIO-mix workload was used to represent them. Using the same IO test, these workloads would now use the AVERAGE RNI LSPR workload. Workloads with higher IO rates may use the HIGH RNI workload or the AVG-HIGH RNI workload that is included with zPCR.

For z10 and newer processors, the CPU MF data may be used to provide a more accurate workload selection. When available, this data allows the RNI for a production workload to be calculated. Using the RNI and another value from CPU MF, the L1 cache misses per 100 instructions, a workload may be classified as LOW, AVERAGE or HIGH RNI. This classification and resulting workload selection is automated in the zPCR tool. It is highly recommended to use zPCR for capacity sizing. For those wanting to perform the workload selection by hand, the following table may be used for z10, z196 and zEC12 (note L1MP stands for L1 misses per 100 instructions and is a value that may be calculated using the CPU MF counters data):

L1MP	RNI	Workload Hint
<3	>= 0.75 < 0.75	AVERAGE LOW
3 to 6	>1.0 0.6 to 1.0 < 0.6	HIGH AVERAGE LOW
>6	>= 0.75 < 0.75	HIGH AVERAGE

Changes In CPU Time by the Effect Of Changes In CEC Utilization



CPU Utilization Effect & Capacity Planning

You can estimate by using IBMs Study For Different Workload Types AND YOU CAN MEASURE !. Sync SMF 70s and SMF 113s….

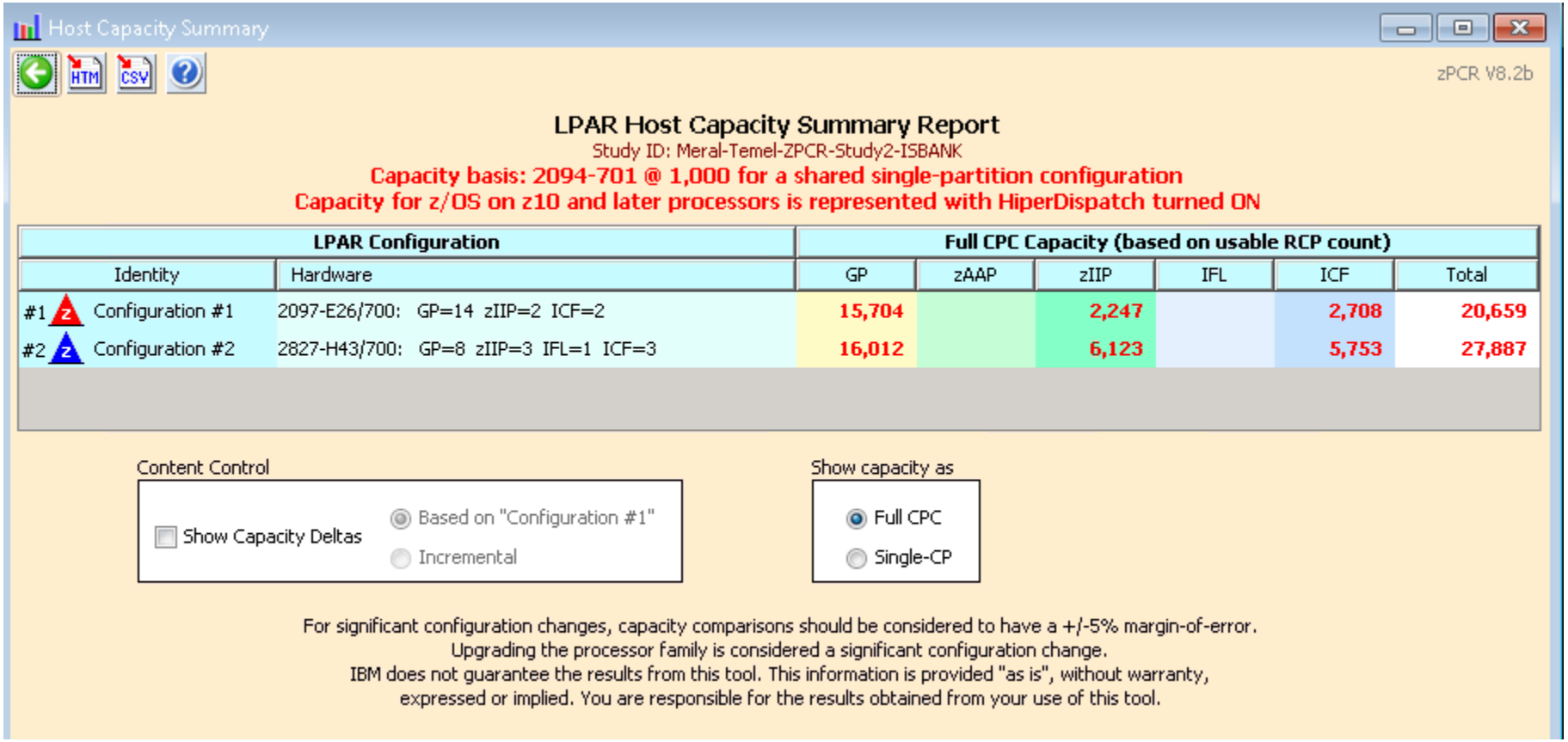
CPU Utilization
Impact to Capacity Planning When Using MIPS

- Impact to capacity planning comes in two flavors
  - may have less headroom on the box than you think
  - when moving a workload, it may not fit in the new container
- Example
  - assume a workload is running at 50% busy on a 2000 MIPS box
    - without factoring in utilization effect, it will be called a 1000 MIPS workload
    - in fact, it may be an 1200 MIPS workload when running at the efficiency of a 90% busy box
  - caution #1: there is NOT room to double this workload on the current box
  - caution #2: if moved to a new box or LPAR, it will likely need a 1200 MIPS container (not 1000 MIPS) to fit
- Estimating the impact - conservative approach
  - For a change in utilization of 10%, plan for the capacity effect to be
    - 3% for LOW RNI workloads
    - 4% for AVERAGE RNI workloads
    - 5% for HIGH RNI workloads

Capacity & PERFORMANCE Planning
LPAR Configuration Planning
ZPCR STUDY

zPCR Is NOT ONLY CAPACITY PLANNING PRODUCT
Please use zPCR!.

zPCR STUDY – ISBANK01 – First CEC – Move From z10 -714 To zEC12- 708



Host Capacity Summary

zPCR V8.2b

LPAR Host Capacity Summary Report

Study ID: Meral-Temel-ZPCR-Study2-ISBANK

Capacity basis: 2094-701 @ 1,000 for a shared single-partition configuration

Capacity for z/OS on z10 and later processors is represented with HiperDispatch turned ON

LPAR Configuration		Full CPC Capacity (based on usable RCP count)					
Identity	Hardware	GP	zAAP	zIIP	IFL	ICF	Total
#1 Configuration #1	2097-E26/700: GP=14 zIIP=2 ICF=2	15,704		2,247		2,708	20,659
#2 Configuration #2	2827-H43/700: GP=8 zIIP=3 IFL=1 ICF=3	16,012		6,123		5,753	27,887

Content Control

Show Capacity Deltas

Based on "Configuration #1"

Incremental

Show capacity as

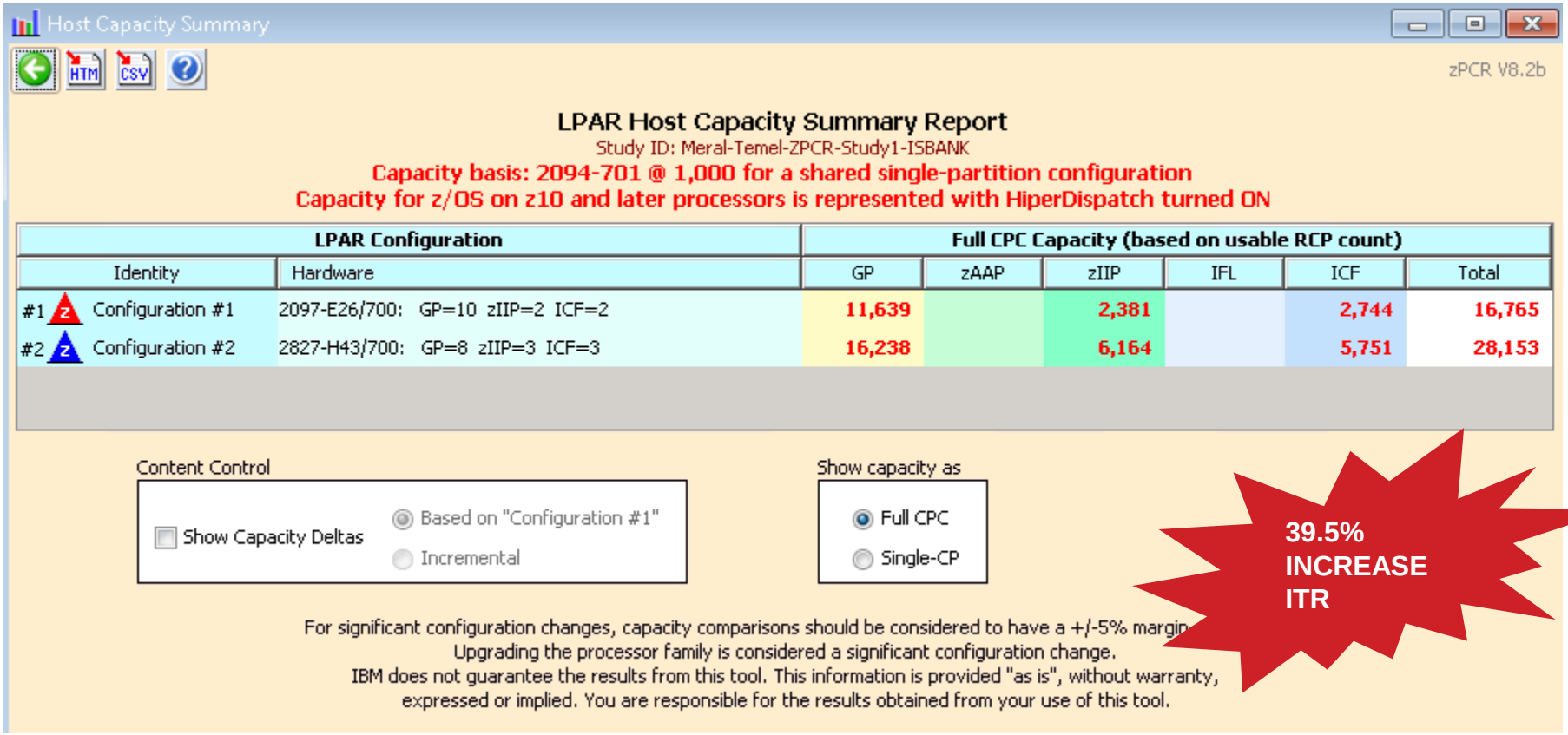
Full CPC

Single-CP

For significant configuration changes, capacity comparisons should be considered to have a +/-5% margin-of-error.
Upgrading the processor family is considered a significant configuration change.
IBM does not guarantee the results from this tool. This information is provided "as is", without warranty,
expressed or implied. You are responsible for the results obtained from your use of this tool.

Only 1.9% ITR Increase

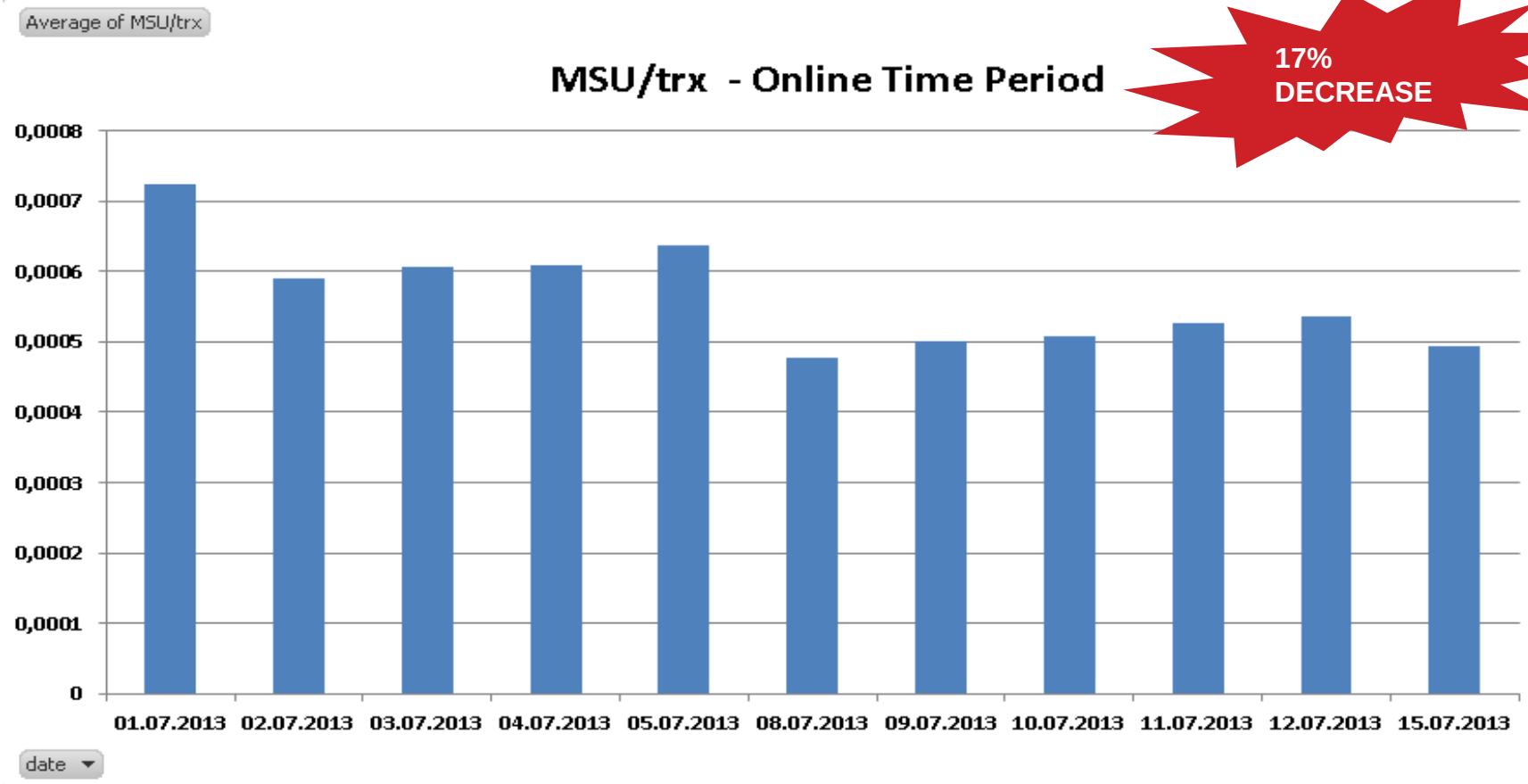
zPCR STUDY – ISBANK02 – Second CEC – Move From z10 -710 To zEC12- 708



SHARE zPCR LAB Sessions – John Burg

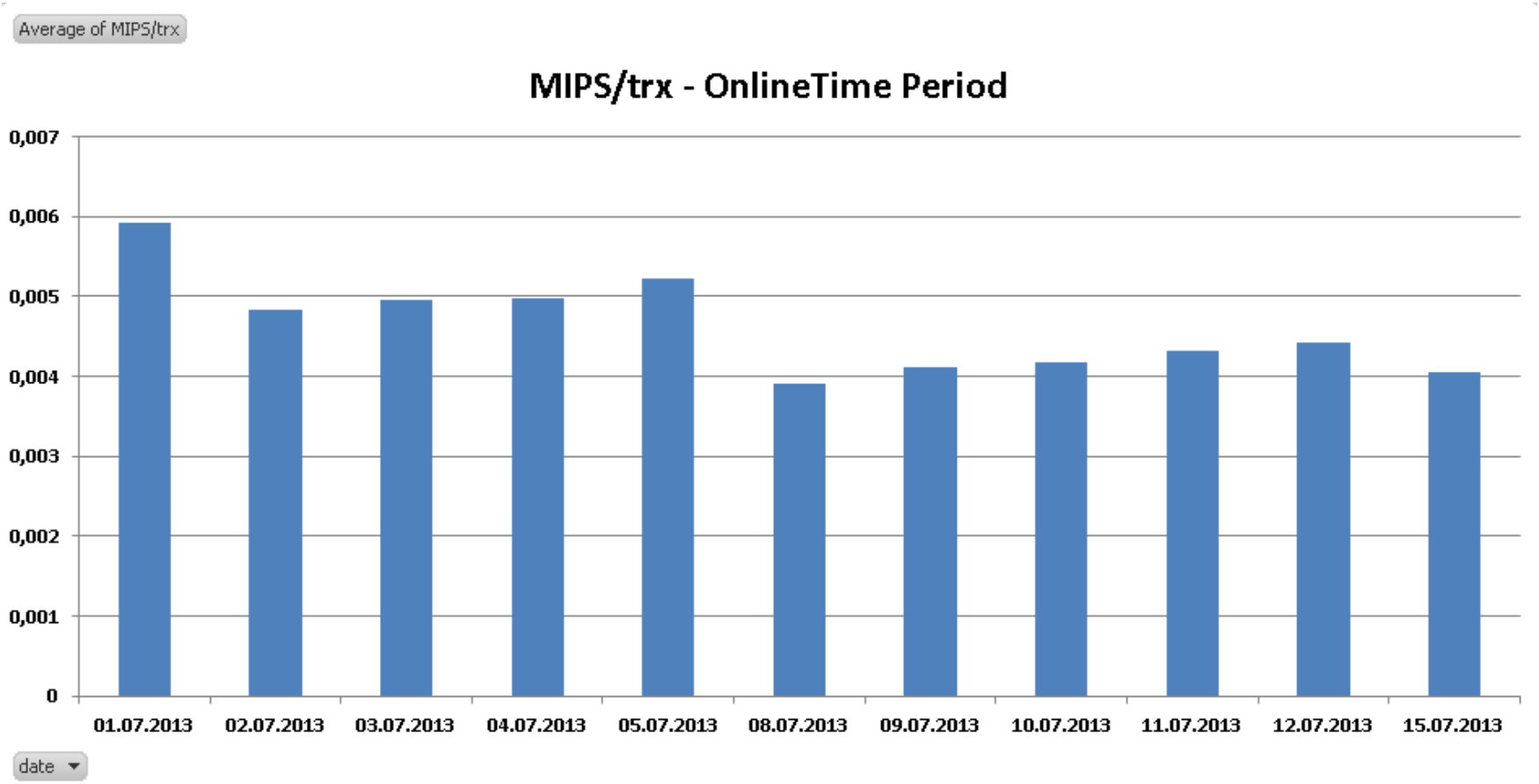
Effect Of CPU Efficiency To MSUs Consumed

= (Sum of All 15 minute Interval IMS Regions APPL% between 09:00 & 18:00) X (MSU/CP)
Sum of # Of IMS Transactions Processed



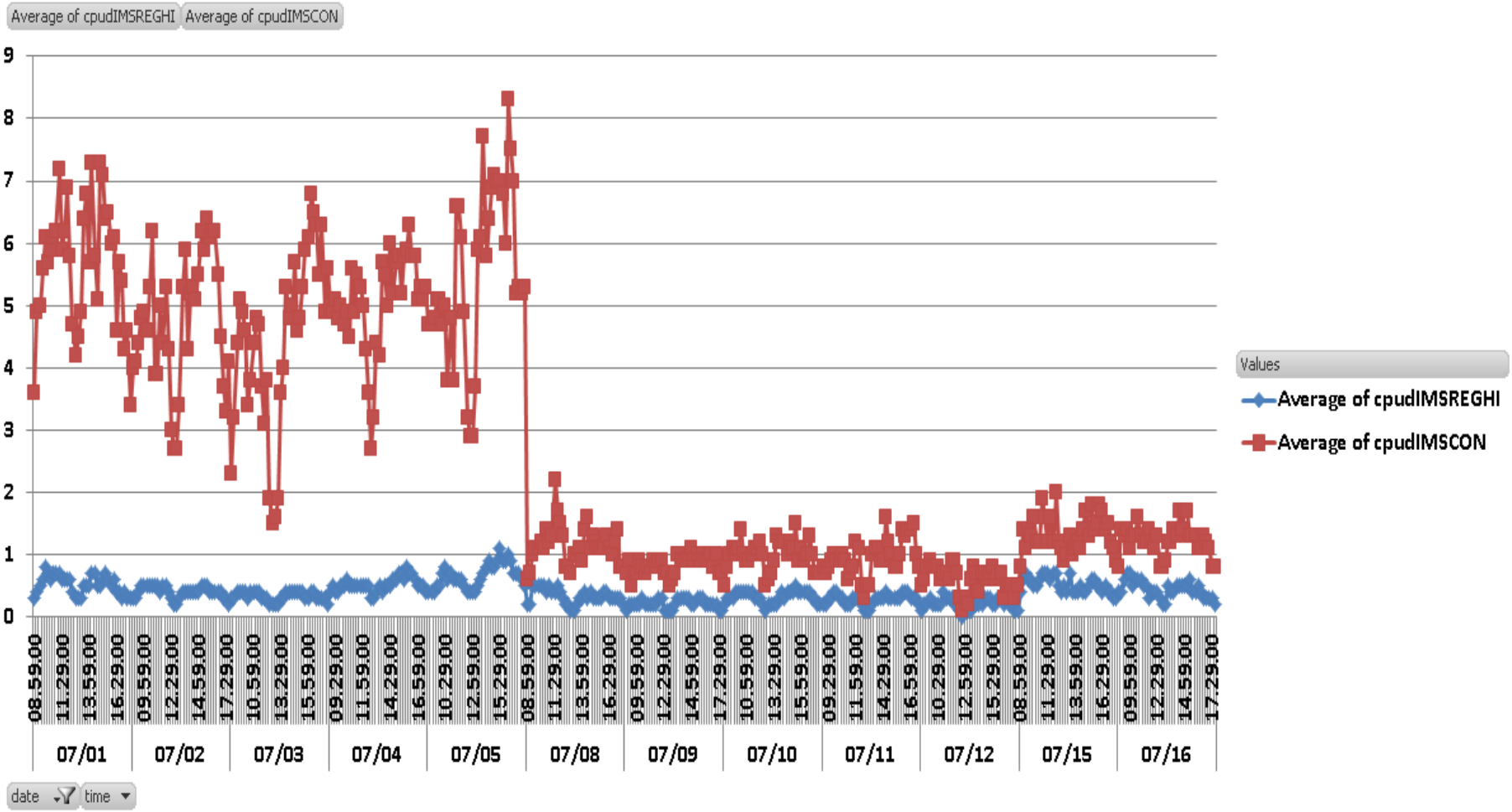
Effect Of CPU Efficiency To MIPS Consumed

$$= \frac{\text{(Sum of All 15 minute Interval IMS Regions APPL\% between 09:00 \& 18:00) X (MIPS/CP)}}{\text{Sum of \# Of IMS Transactions Processed}}$$



Effect to CPU Delays Of IMS Regions

CPU Delay % Of SYSA -IMS –IREGHI Service Class
CPU Delay % Of SYSA- IMSConnect Address Space Service Class

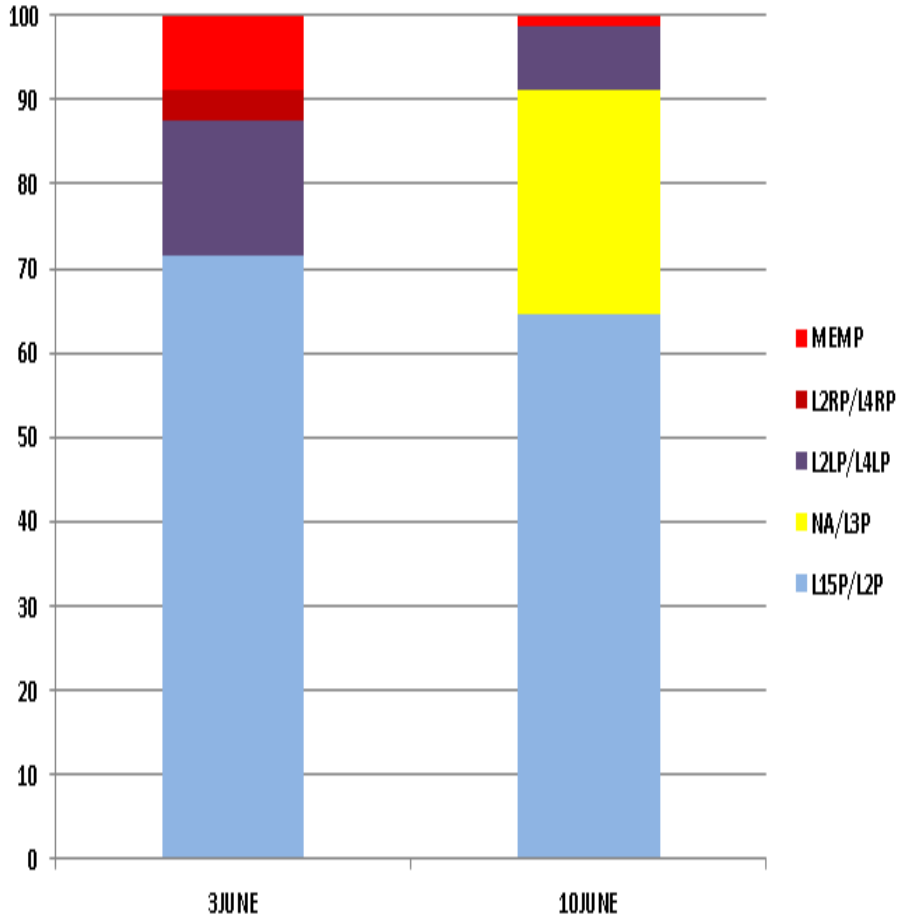


SMF113 Study - SYSY System

10 JUNE / 3 JUNE SYSY ONLINE WORKLOAD TIME (09:00-18:00) COMPARISON

Cycle Per Instruction Decreased By %49

DATE	3JUNE	10JUNE	DECREASE%
CPI	7,46	3,81	49
L1MP	4,26	4,85	
L15P	71,58	NA	
L2P	NA	64,48	
L2LP	15,90	NA	
L2RP	3,84	NA	
L3P	NA	26,58	
L4LP	NA	7,74	
L4RP	NA	0,03	
LPARBUSY	7,89	54,67	
MEMP	8,68	1,16	87
MIPSEXEC	46,73	791,00	
ESTICCPI	3,07	2,10	32
ESTFINCP	4,40	1,71	61
ESTSCP1M	103,40	35,23	66
RNI	0,90	0,65	
EFFGHZ	4,40	5,50	
TLB1MISS	8,10	5,62	31
TLB1CYCL	79,49	27,28	66
PTEPCTMI	36,74	27,57	25



SMF113 Study - SYSA & SYSB System

%40 DECREASE In CPI (Cycle Per Instruction) = THIS IS OUR MIPS that we gain back!

	SYSA	SYSA	
ITEM	10JUNE	8JULY	%DECREASE
CPI	7,79	4,62	40,6
L1MP	4,91	5,60	
L15P/L2P	71,07	64,10	9,8
L2LP/L4LP	21,82	7,11	67,4
L2RP/L4RP	3,07	0,44	85,5
L3P		27,14	
LPARBUSY	53,23	335,97	
MEMP	4,04	1,21	70,2
MIPSEXEC	301,53	3999,24	
ESTICCPI	4,02	2,55	36,5
ESTFINCP	3,76	2,07	44,9
ESTSCP1M	76,74	37,10	51,6
RNI	0,60	0,67	
EFFGHZ	4,40	5,50	
TLB1MISS	6,07	6,20	
TLB1CYCL	55,47	33,73	39,2
PTEPCTMI	35,26	37,01	

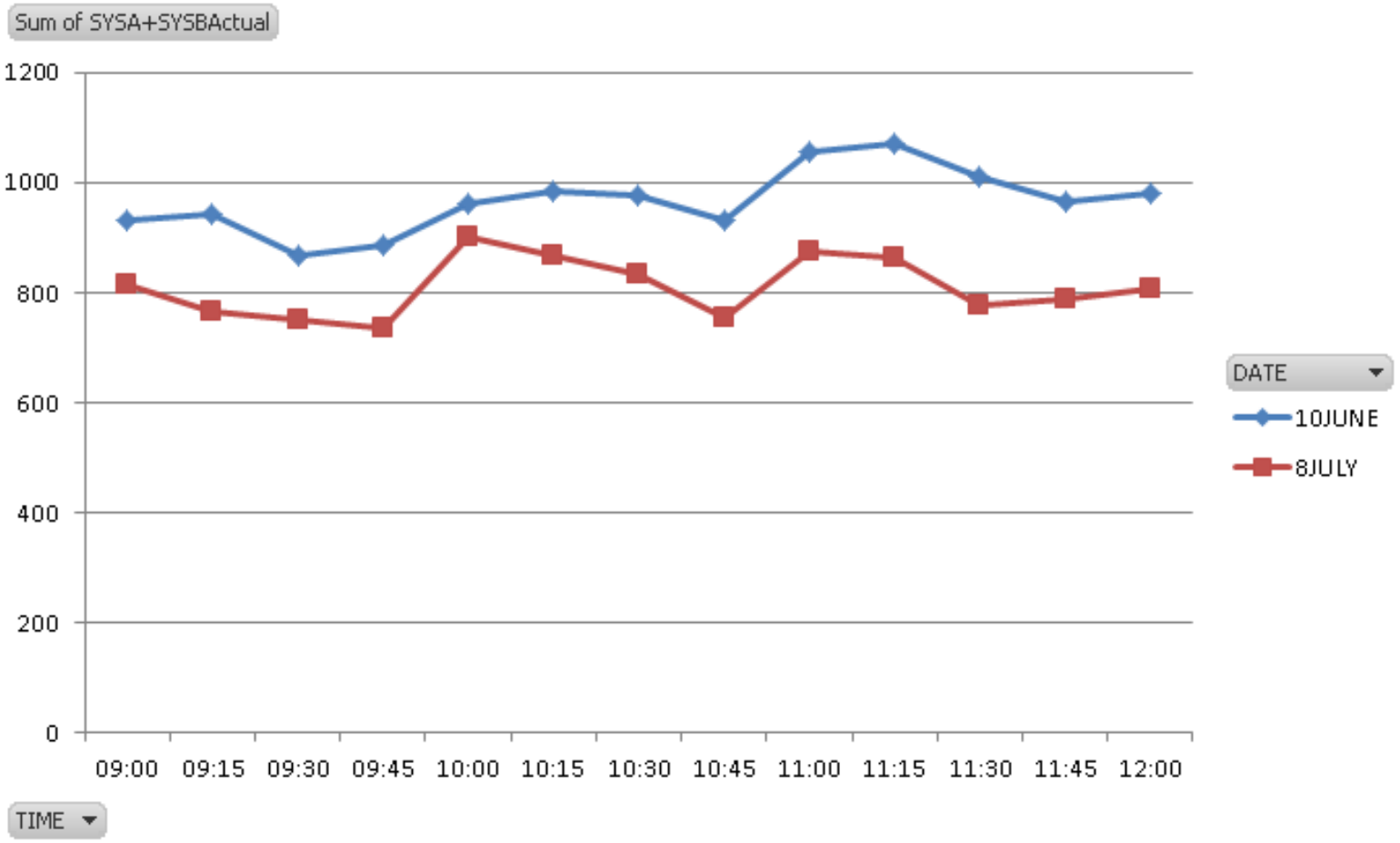
	SYSB	SYSB	
ITEM	10JUNE	8JULY	%DECREASE
CPI	8,12	4,35	46,4
L1MP	5,23	5,13	
L15P/L2P	72,74	66,87	8,1
L2LP/L4LP	22,63	4,93	78,2
L2RP/L4RP	0,09	0,13	
L3P		27,01	
LPARBUSY	40,58	191,48	
MEMP	4,55	1,07	76,5
MIPSEXEC	220,07	2436,59	
ESTICCPI	4,35	2,73	37,2
ESTFINCP	3,77	1,62	56,9
ESTSCP1M	72,06	31,73	56,0
RNI	0,57	0,57	
EFFGHZ	4,40	5,50	
TLB1MISS	6,06	5,66	
TLB1CYCL	54,65	31,04	43,2
PTEPCTMI	36,13	32,17	

SYSA & SYSB MSU Decrease

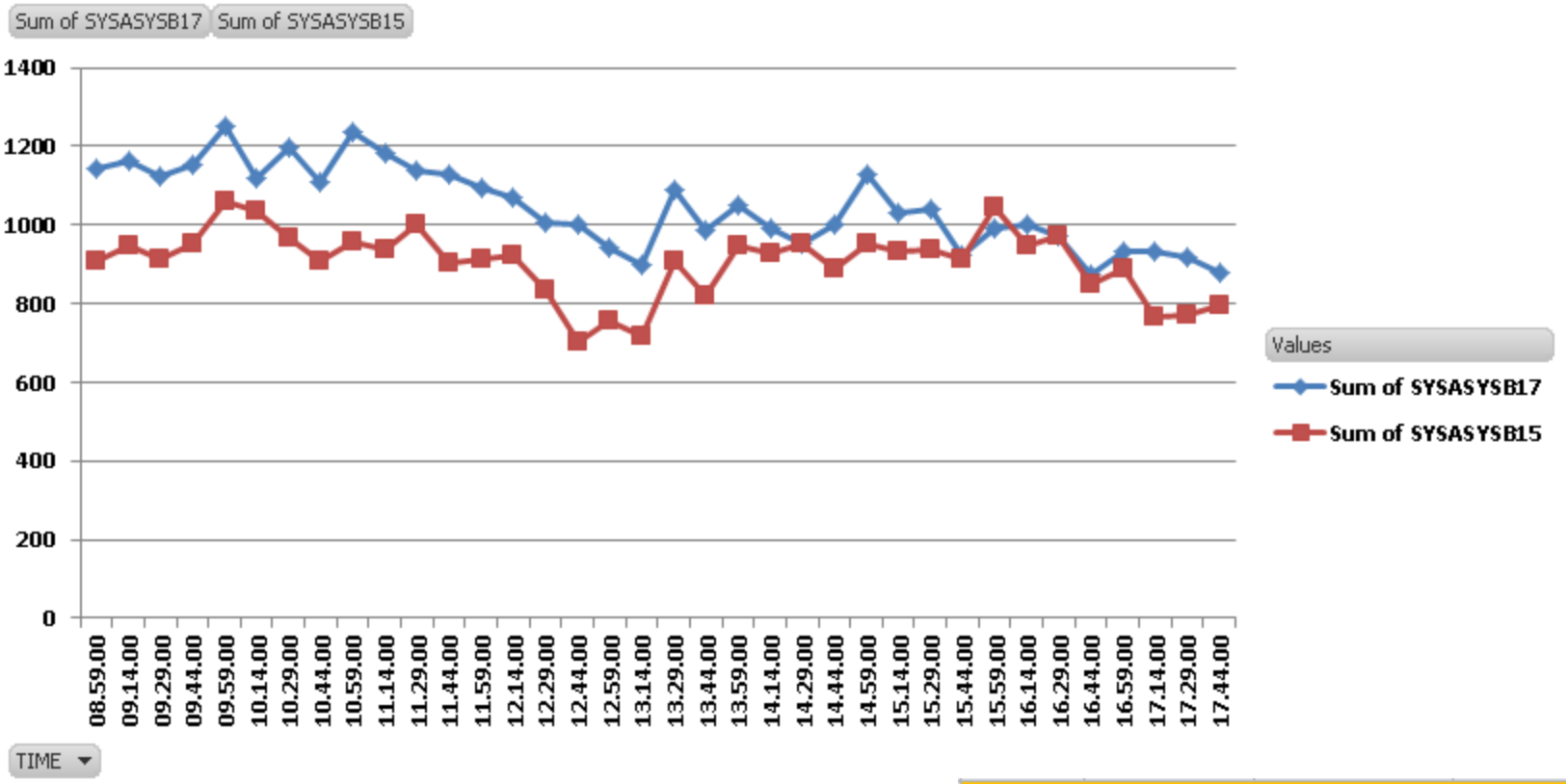
%14 - %23 Decrease In MSU for nearly same amount of Workload

											SYSA+SYSBActual						
DATE	TIME	SYSAactualMSU	dayaverage	decrease%	DATE	TIME	SYSBactualMSU	DATE	TIME	SYSA+SYSBActu	dayaverag	decrease%			Time	IntervalComparison	
8JULY	09:00	490	516		8JULY	09:00	326	8JULY	09:00	816	810				09:00	12,35	
8JULY	09:15	483			8JULY	09:15	281	8JULY	09:15	764					09:15	18,81	
8JULY	09:30	504			8JULY	09:30	248	8JULY	09:30	752					09:30	13,26	
8JULY	09:45	481			8JULY	09:45	254	8JULY	09:45	735					09:45	16,95	
8JULY	10:00	580			8JULY	10:00	322	8JULY	10:00	902					10:00	6,14	
8JULY	10:15	565			8JULY	10:15	301	8JULY	10:15	866					10:15	11,99	
8JULY	10:30	524			8JULY	10:30	310	8JULY	10:30	834					10:30	14,55	
8JULY	10:45	476			8JULY	10:45	278	8JULY	10:45	754					10:45	18,92	
8JULY	11:00	555			8JULY	11:00	318	8JULY	11:00	873					11:00	17,41	
8JULY	11:15	564			8JULY	11:15	301	8JULY	11:15	865					11:15	19,31	
8JULY	11:30	498			8JULY	11:30	278	8JULY	11:30	776					11:30	23,09	
8JULY	11:45	485			8JULY	11:45	302	8JULY	11:45	787					11:45	18,53	
8JULY	12:00	503			8JULY	12:00	305	8JULY	12:00	808					12:00	17,72	
10JUNE	09:00	552	605	14,7	10JUNE	09:00	379	10JUNE	09:00	931	966	16,2	12,35				
10JUNE	09:15	569			10JUNE	09:15	372	10JUNE	09:15	941			18,81				
10JUNE	09:30	495			10JUNE	09:30	372	10JUNE	09:30	867			13,26				
10JUNE	09:45	535			10JUNE	09:45	350	10JUNE	09:45	885			16,95				
10JUNE	10:00	587			10JUNE	10:00	374	10JUNE	10:00	961			6,14				
10JUNE	10:15	615			10JUNE	10:15	369	10JUNE	10:15	984			11,99				
10JUNE	10:30	595			10JUNE	10:30	381	10JUNE	10:30	976			14,55				
10JUNE	10:45	591			10JUNE	10:45	339	10JUNE	10:45	930			18,92				
10JUNE	11:00	699			10JUNE	11:00	358	10JUNE	11:00	1057			17,41				
10JUNE	11:15	679			10JUNE	11:15	393	10JUNE	11:15	1072			19,31				
10JUNE	11:30	639			10JUNE	11:30	370	10JUNE	11:30	1009			23,09				
10JUNE	11:45	637			10JUNE	11:45	329	10JUNE	11:45	966			18,53				
10JUNE	12:00	667			10JUNE	12:00	315	10JUNE	12:00	982			17,72				

SYSA & SYSB MSU Decrease

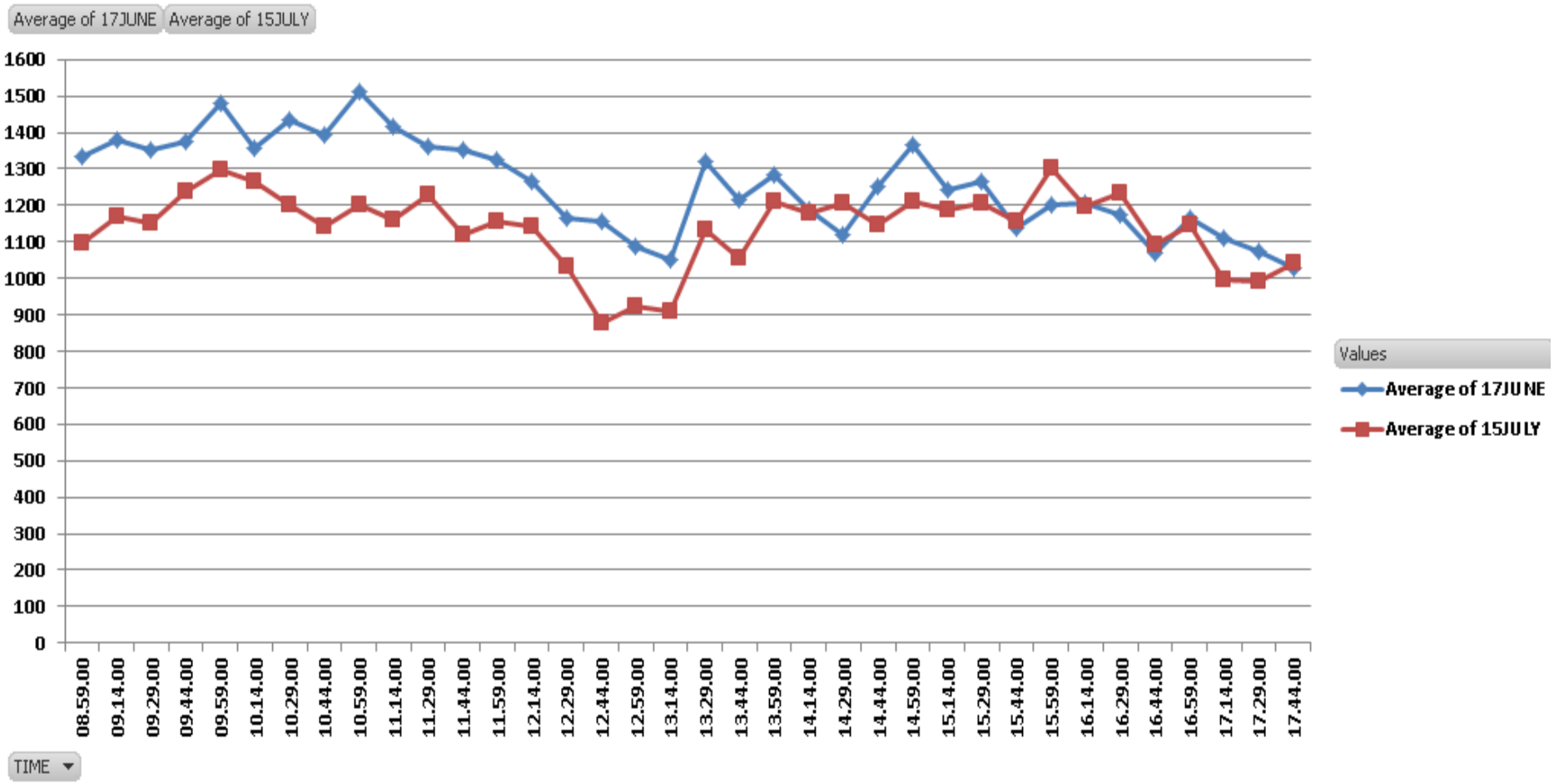


Peak Day SYSA & SYSB MSU Decrease %15 Although 15 July Is The Record Breaking Day For # Of Transactions



SYSA & SYSB TOTAL ACTUAL MSU (Average)			
PERIOD	17June	15July	%DIFFERENCE
09-12	1395	1189	85
14-18	1180	1157	98

Peak Day SYSA & SYSB MSU Decrease %15 Although 15 July Is The Record Breaking Day For # Of Transactions



IMSCON Address Spaces' Service Units & CpuTime

TIME	TOTAL-SU-10June	TOTAL-SU-8July	%DIFFERENCE
09:00	6040549	5096530	15,63
09:15	6812501	5966145	12,42
09:30	7108471	6565781	7,63
09:45	7379635	7024891	4,81
10:00	8010046	7653798	4,45
10:15	8200481	7785963	5,05
10:30	8026827	7583087	5,53
10:45	8213571	7536075	8,25
11:00	9466314	7924118	16,29
11:15	9049287	7778164	14,05
11:30	9016012	7740987	14,14
11:45	8694807	7617411	12,39

IMSCON AS CPUTIME (in seconds)			
time	tot10june	tot8july	%DECREASE
09:00	173,867	79,391	54,3
09:15	196,31	92,095	53,1
09:30	204,125	101,352	50,3
09:45	211,709	108,445	48,8
10:00	230,696	118,147	48,8
10:15	237,257	120,199	49,3
10:30	232,276	117,059	49,6
10:45	237,786	116,338	51,1
11:00	274,394	122,338	55,4
11:15	261,751	120,075	54,1
11:30	261,421	119,493	54,3
11:45	252,42	117,595	53,4
12:00	256,096	118,286	53,8

IBM WSC – JOHN BURG's ANALYSIS Special Thanks To John Burg For This Study

zPCR used to set Expectations based on actual configuratio

- **Accuracy of zPCR is within +/- 5%**
  - Measurement is Average for all workloads
  - Capacity Levels set with z9-701 set to 593 MIPS

Processor 1

	z10 714	zEC12 708	Relative Capacity Ratio
MIPS	9,313.0	9,495.0	
GCP Engir	14	8	
MIPS / Eng	665.0	1187.0	1.78

Processor 2

	z10 710	zEC12 708	Relative Capacity Ratio
MIPS	6,902.0	9,629.0	
GCP Engir	10	8	
MIPS / Eng	690.0	1204.0	1.74

zEC12-708 Processor 1 Performance Vs Expectation

Overall the zEC12 appears to be performing above expectations by 22% to 23%

Prime 9 AM to Noon

																		Measured LPARs Weighted Actual "After"		Measured LPARs Weighted		
			Median	AVG IRATE	Median	Avg CPU	Avg GCP	Median	zPCR GCP	Measured LPARs Median GCP ITR			Weighted LPARs Median GCP ITR Vs	DASD	DASD I/O		Weighted Actual zEC12	Actual GCP CPI	Weighted Actual CPI
zEC12-708	LPAR	AVG GCP CPI	GCP CPI	ITR	IRATE ITR	ITR	ITR	GCP ITR	Expectation	Vs Expectation	LPAR CPU	% Total LPAR CPU	Expectation	SSCHs	Resp		IRATE ITR Vs Expectation	ITR Vs Expectation	ITR Vs Expectation
	SYSA	2.15	2.20	2.25	2.23	2.24	2.24	2.22	1.78	1.25	302.8	100.0%	1.25	0.90	0.95		1.26	1.25	1.23	1.23
	SYSY	0.95	0.94	1.06	1.04	1.41	1.24	1.18	1.00	1.18	0.0	0.0%	0.00	0.82	0.84		1.04	0.00	0.94	0.00
	Avg/Sum ==>		1.67	1.66	1.63		1.74	1.70			302.8	100.0%	1.25	0.86	0.89		1.16	1.25	1.09	1.23
											42.8									

zEC12 Box Lower Utilization Amount Vs z10 - "Low" workload: 4.9%

Lower Utilization Effect (LUE) Factor: Average 0.985 | 0.985 | 0.985

LUE Adjusted Weighted Actual zEC12 GCP ITR Vs Expectation: 1.23 | 1.23 | 1.22

zEC12-708 Processor 2 Performance Vs Expectation

Overall the zEC12 appears to be performing above expectations by 15% to 26%

Prime 9 AM to Noon

	SMF 113	SMF 113	SMF 70x	SMF 70x	SMF 72x	zPCR GCP Expectation	SMF 72x	SMF 70x	SMF 113	SMF 113
LPAR	AVG GCP CPI	Median GCP CPI	AVG IRATE ITR	Median IRATE ITR	Avg CPU ITR	Avg GCP ITR	Median GCP ITR	zPCR GCP Expectation	Measured LPARs Median GCP ITR Vs Expectation	LPAR CPU	% Total LPAR CPU	Weighted LPARs Median GCP ITR Vs Expectation	DASD SSCHs	DASD I/O Resp	Measured LPARs Weighted Actual "After" IRATE ITR Vs Expectation	Weighted Actual zEC12 IRATE ITR Vs Expectation	Measured LPARs Weighted Actual GCP CPI ITR Vs Expectation	Weighted Actual CPI ITR Vs Expectation
SYSB	2.30	2.30	2.09	2.04	2.15	2.14	2.09	1.74	1.20	200.8	76.4%	0.92	1.12	1.03	1.17	0.89	1.32	1.01
SYSZ	0.00	2.12	2.20	2.17	2.21	2.17	1.99	1.74	1.14	62.2	23.6%	0.27	1.20	1.16	1.25	0.30	1.22	0.29
Avg/Sum ==>		2.21	2.14	2.10		2.16	2.04			263.0	100.0%	1.19	1.16	1.10	1.21	1.19	1.27	1.30
											zEC12 Box Lower Utilization Amount Vs z10 - "Low" workload	Lower Utilization Effect (LUE) Factor						
Average											10.2%	0.970				0.970		0.970
LUE Adjusted Weighted Actual zEC12 GCP ITR Vs Expectation												1.15				1.15		1.26

Performance Summary Vs zPCR Expectations

- **Summary**
  - Both zEC12s appear to be performing better than expectations
    - zEC12 Processor 1 by 22% to 23%
    - zEC12 Processor 2 by 15% to 26%
    - As suggested by 3 independent metrics SMF 70s, SMF 72s and SMF 113s

	SMF 72 GCP ITR Vs Expectation	SMF 70 IRATE ITR Vs Expectation	SMF 113 CPI ITR Vs Expectation
zEC12-708 SYSA	1.23	1.23	1.22
zEC12-708 SYSB / SYSZ	1.15	1.15	1.26
zPCR Expectation	1.00		

CPU MF Characteristics - SYSA

SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L15P / L2P	L3P	L2LP / L4LP	L2RP / L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	Machine Type	LSPR Wkld
zEC12-708																				
Prime 9 AM to Noon																				
SYSA																				
SYSA	JUN	17	P	TOTA	7.96	0.0	3.91	4.06	84	4.8	69.4	0.0	22.5	3.4	4.8	0.67	962.9	4.4	Z10	AVG
SYSA	JUN	18	P	TOTA	8.25	0.0	4.52	3.72	74	5.0	71.6	0.0	21.6	3.2	3.7	0.57	732.9	4.4	Z10	LOW
SYSA	JUN	19	P	TOTA	7.40	0.0	3.80	3.60	73	4.9	72.1	0.0	21.2	3.1	3.6	0.56	688.6	4.4	Z10	LOW
z10 Average					**7.87**	**0.0**	**4.08**	**3.79**	**77**	**4.9**	**71.0**	**0.0**	**21.8**	**3.2**	**4.0**	**0.60**	**794.8**			

SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L15P / L2P	L3P	L2LP / L4LP	L2RP / L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	Machine Type	LSPR Wkld
SYSA	JUL	8	P	TOTA	4.65	0.0	2.58	2.07	36	5.8	64.9	26.7	6.8	0.5	1.1	0.64	317.5	5.5	ZEC12	AVG
SYSA	JUL	9	P	TOTA	4.53	0.0	2.60	1.93	34	5.7	65.5	27.1	6.1	0.5	1.0	0.60	286.0	5.5	ZEC12	AVG
SYSA	JUL	10	P	TOTA	4.53	0.0	2.56	1.97	35	5.7	65.2	27.3	6.1	0.5	1.1	0.62	285.5	5.5	ZEC12	AVG
SYSA	JUL	15	P	TOTA	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
zEC12 Average					**4.57**	**0.0**	**2.58**	**1.99**	**35**	**5.7**	**65.2**	**27.0**	**6.3**	**0.5**	**1.0**	**0.62**	**296.3**			
Relative Capacity Ratio					**2.15**		**0.63**			**1.16**					**0.26**					

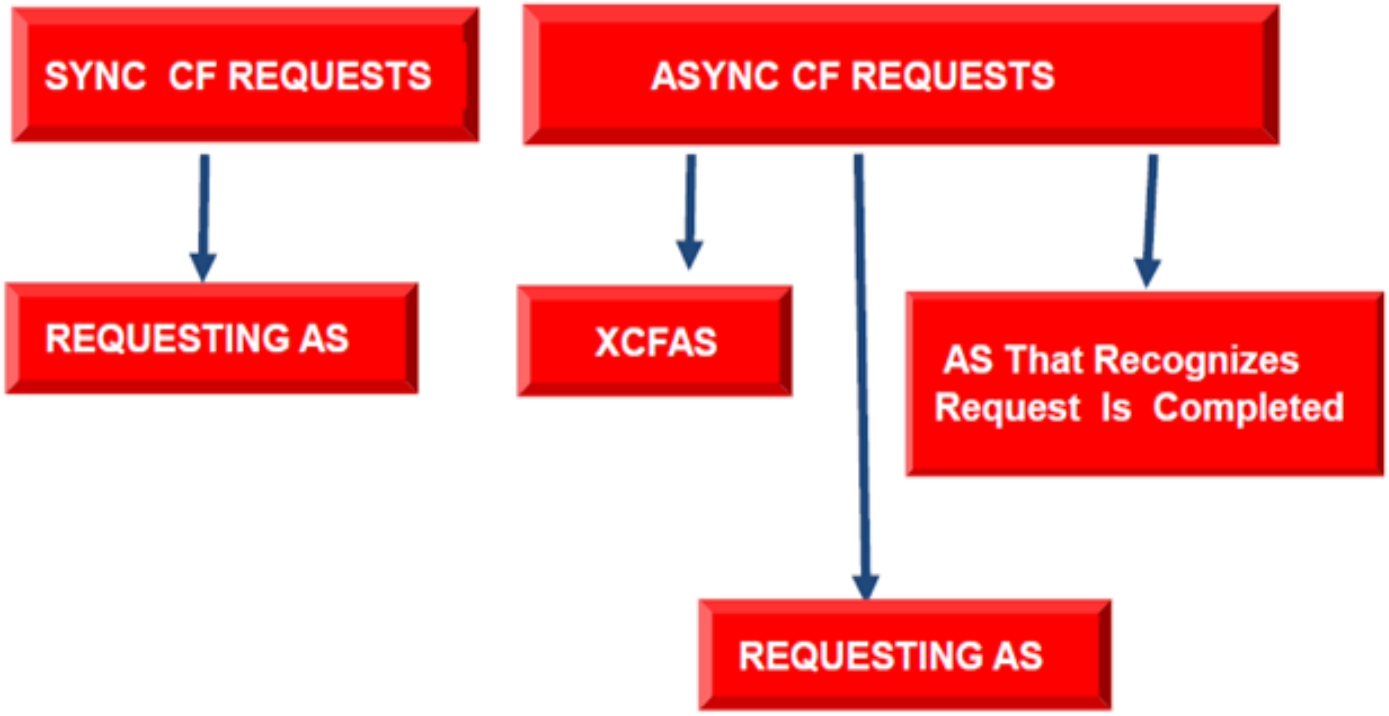
- **RNI metric is consistent between Processors .60 Vs .62**

Observations

- **Observations**
  - Both zEC12s appear to be performing better than expectations
    - zEC12 Processor 1 by 22% to 23%
    - zEC12 Processor 2 by 15% to 26%
  - RNI metrics are consistent across 2 processor generations
    - SYSA and SYSB
  - IS Bank benefitted from zEC12 Processor Architecture Vs z10
    - GHz, Larger Caches and Enhanced Out-Of-Order Execution

HOW IS MY CF WORKLOAD EFFECTED ?
CF VIEW

CF REQUEST TYPES



Sync/Async Conversion

NON-HEURISTIC

- Subchannel Busy Condition
- Path Busy Condition
- Serialized List or Lock Contention

HEURISTIC

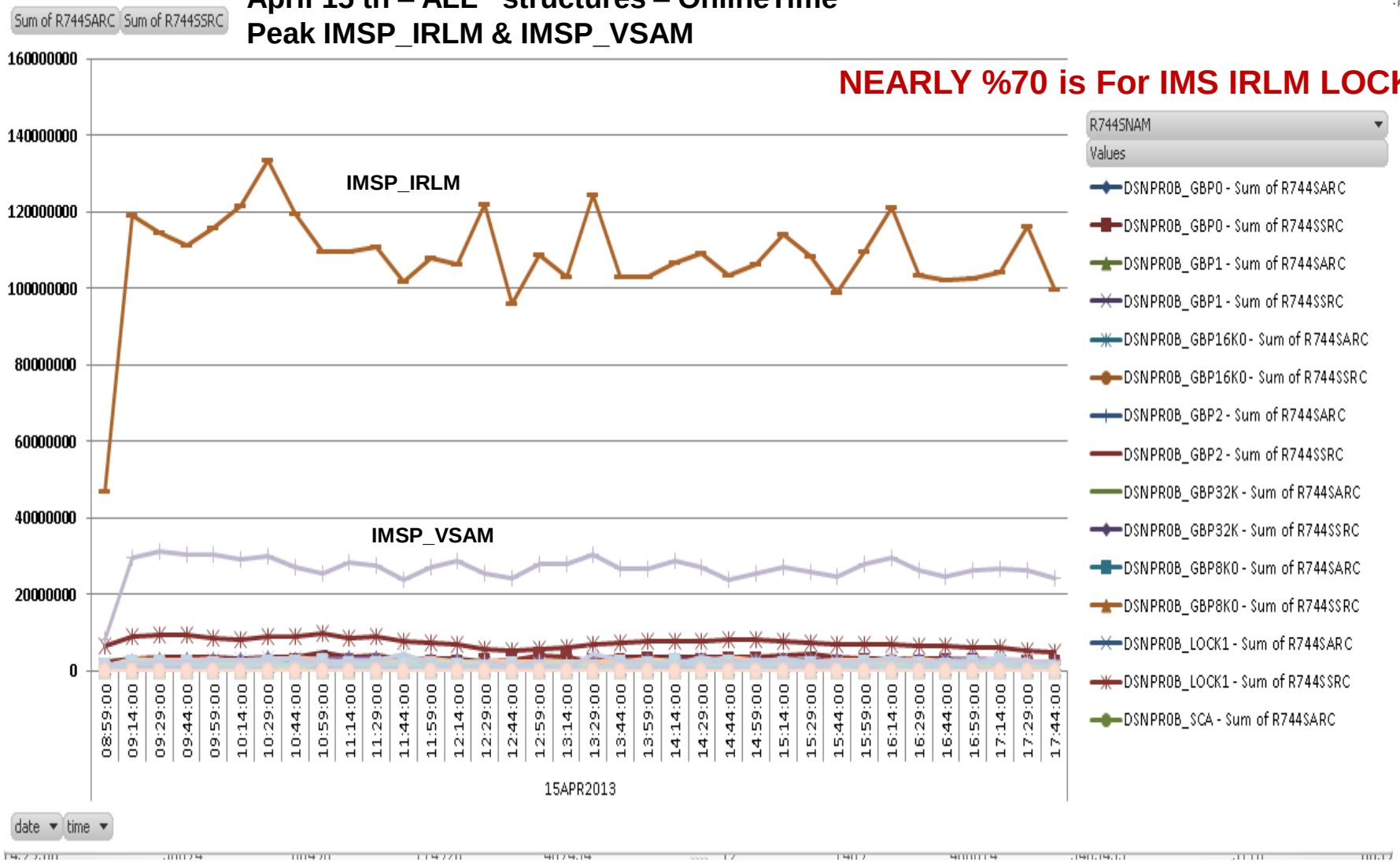
Introduced with z/OS v1r2...

- CF Link Technology
- Types Of Workload – Variable Workload Amount
- Range Of CF Utilization,Shared CP or not,...
- Actual Observed Sync Request Service Time
- Amount Of Data That Needs To Be Transfered
- Other items that effect CF response ex:Distance
- Moving Weighted Averages Of Actual CF Requests
- Every 1 of N Request not converted and send as Sync

OUR CF WORKLOAD CHARACTERISTICS

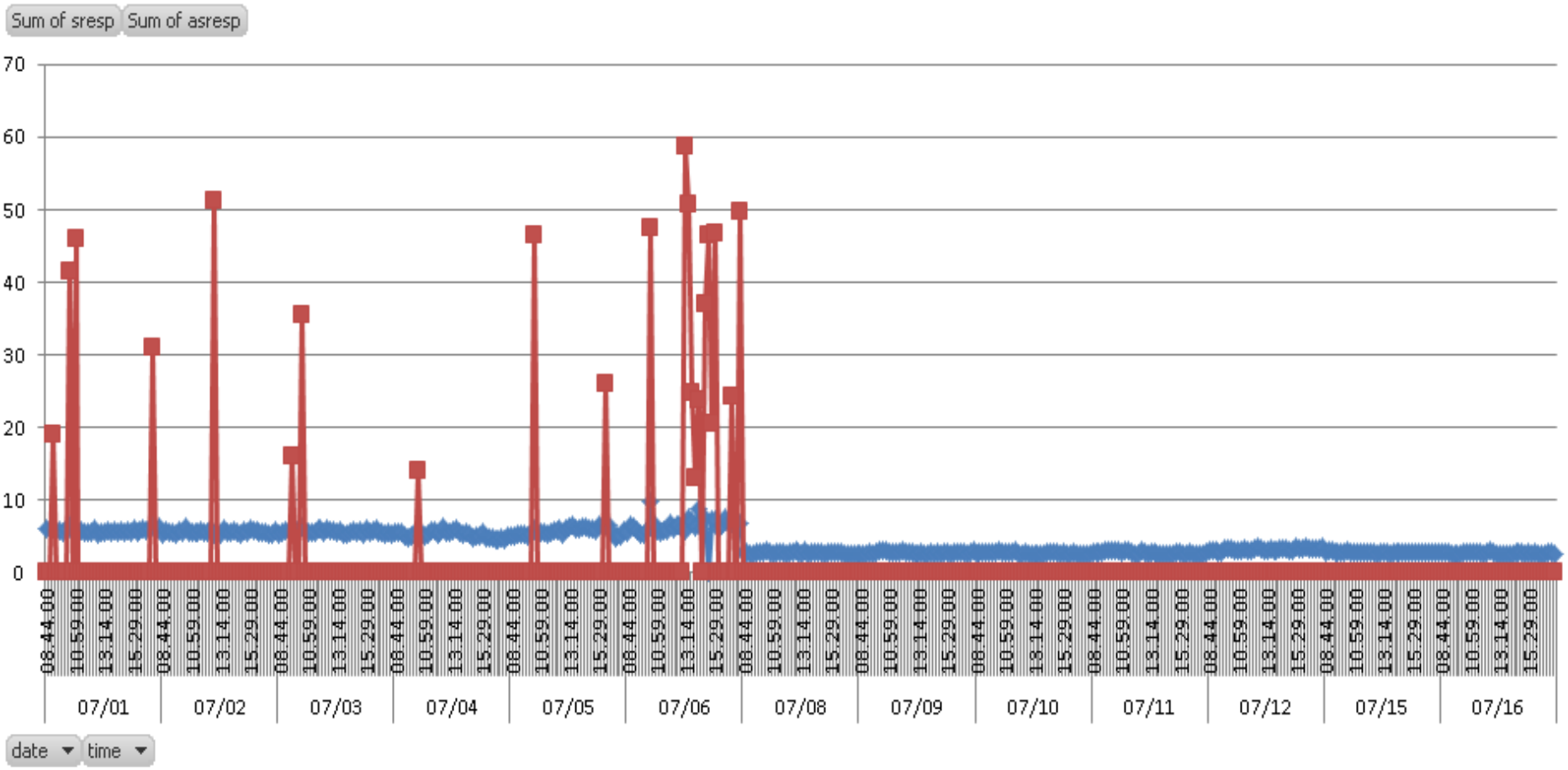
Structures Characteristics – Usage
April 15 th – ALL structures – OnlineTime
Peak IMSP_IRLM & IMSP_VSAM

NEARLY %70 is For IMS IRLM LOCK



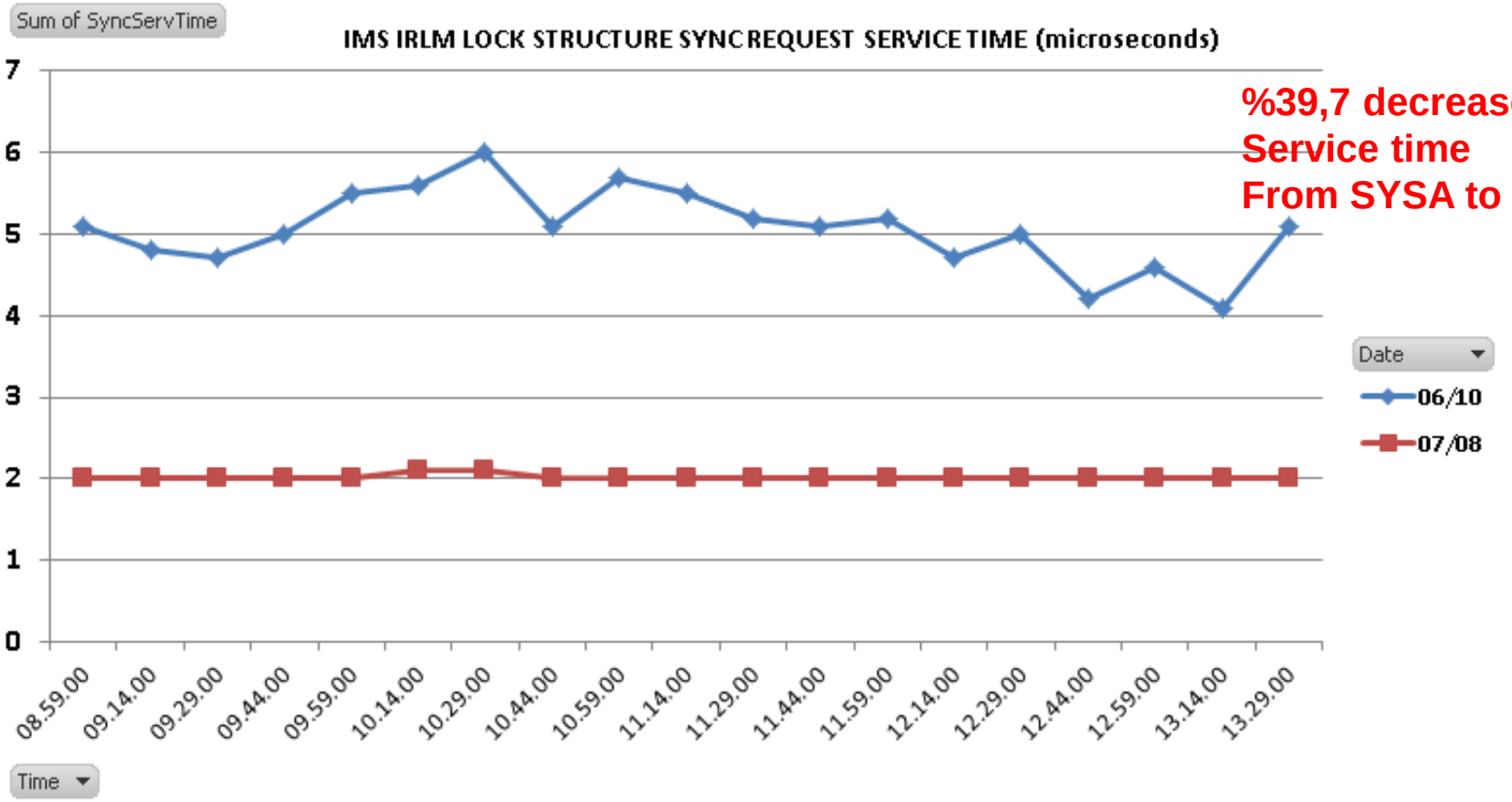
Effect to CF Request Service Times for IMS IRLM Lock Structure

Effect to CF Request Service Times for IMS IRLM Lock Structure – Sync Req Service Time & Async Req Service Time (microseconds)



IC Links Performance Improvement
CF Request Service Times for IRLM Lock Structure

Z10 IC Link – ZEC12 IC Link Performance Improvement
This is Seen For IMS Lock Structure Access from SYSA

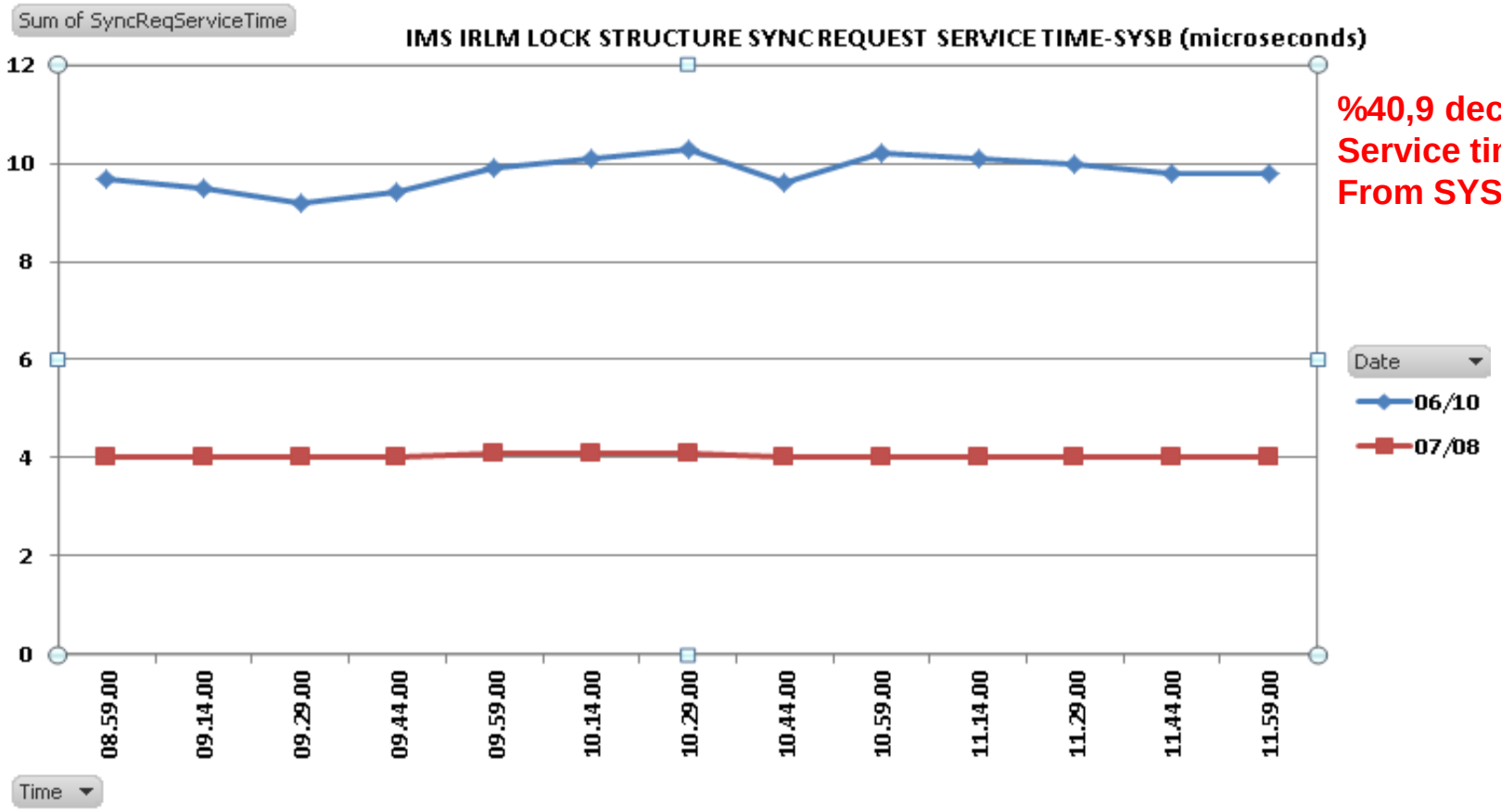


%39,7 decrease in Service time From SYSA to CF Str

CF Processor Speed & 2 ICFs to 3 ICFs (1 CF to 2 CFs for production) increase also causes this result

ICB4 To Infiniband Links Change Effect to Performance CF Request Service Times for IRLM Lock Structure

Z10 2 ICB4 Links – ZEC12 3 Infiniband Links Performance Improvement
This is Seen For IMS Lock Structure Access from SYSB



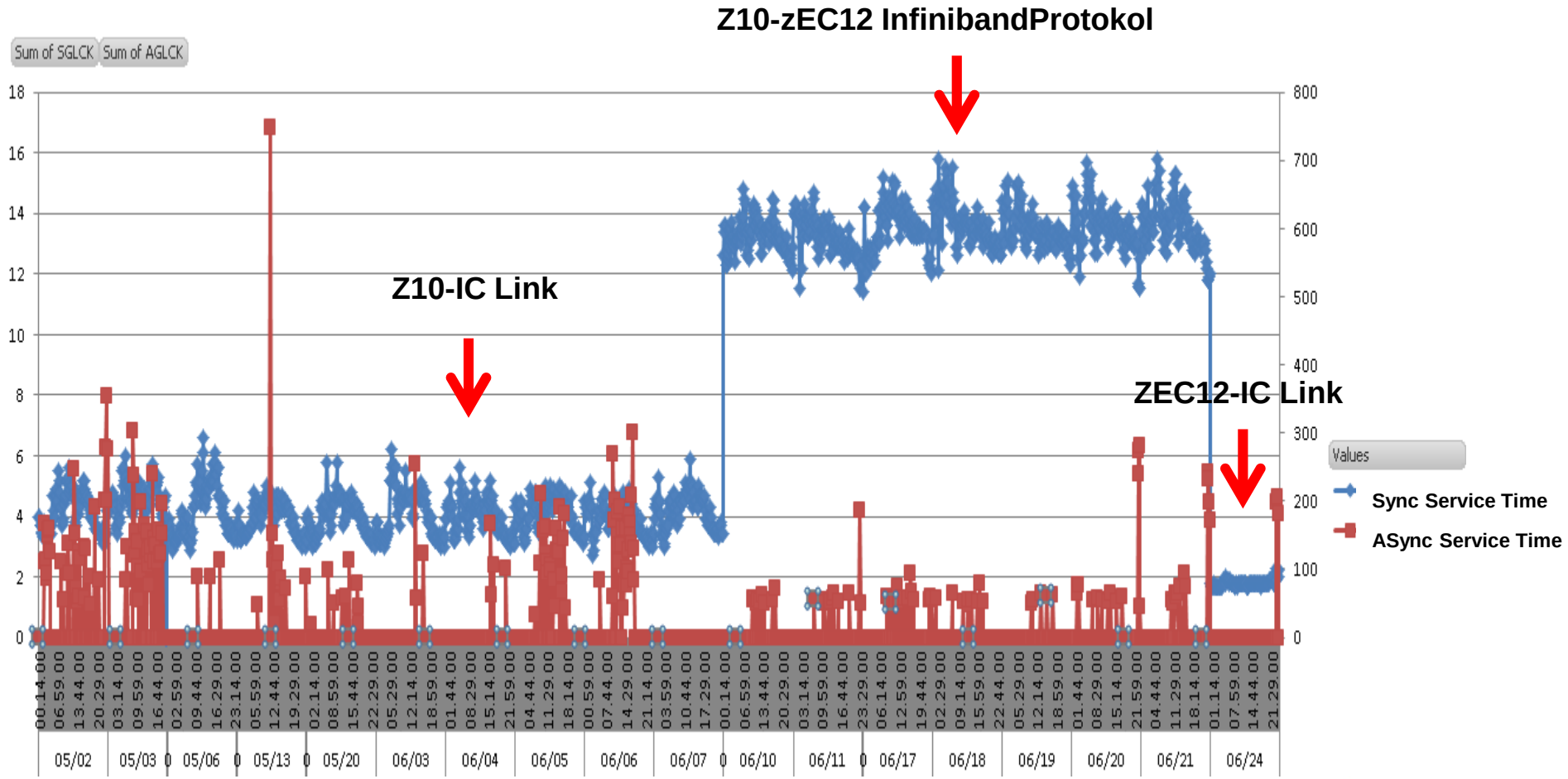
%40,9 decrease in Service time From SYSB to CF Str

CF Processor Speed & 2 ICFs to 3 ICFs (1 CF to 2 CFs for production) increase also causes this result

Effect to CF Request Service Times for DB2 Lock Structure

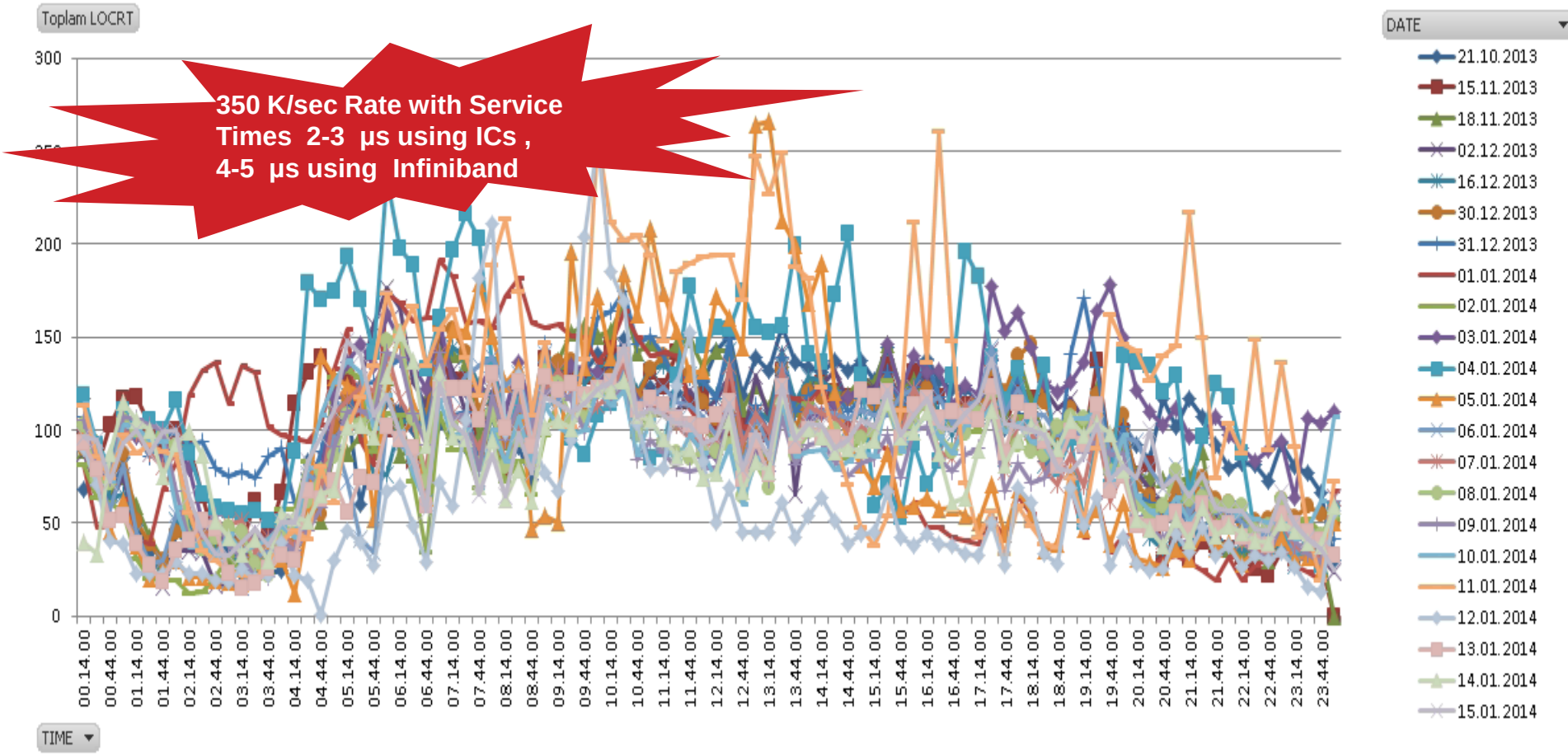
SYSY – DB2 Lock Structure Sync & Async ServiceTime (microseconds)
%50 DECREASED ServiceTime

Because z10 Supports Only Earlier InfinibandProtokol-This Was Something We Have Expected



Excellent CF Service Time Even With 350K/sec CF request rates

15 Min Interval Average IMS Lock Str Request Rate/sec
(In 10 sec interval 350K /sec was reported with 2-4 microseconds responsetimes)



CHANGES IN DATA SHARING COST

DataSharing Cost Value Changes Estimated To Be Changed From %10 To %11

Coupling Technology versus Host Processor Speed

Host effect with primary application involved in data sharing

Chart below is based on 9 CF ops/Mi - may be scaled linearly for other rates

CF\Host	z10 BC	z10 EC	z114	z196	zEnterprise EC12
z10 BC ISC3	16%	18%	17%	21%	24%
z10 BC 1x IFB	13%	14%	14%	17%	19%
z10 BC 12x IFB	12%	13%	13%	15%	17%
z10 BC ICB4	10%	11%	NA	NA	NA
z10 EC ISC3	16%	17%	17%	21%	24%
z10 EC 1x IFB	13%	14%	14%	17%	19%
z10 EC 12x IFB	11%	12%	12%	14%	16%
z10 EC ICB4	10%	10%	NA	NA	NA
z114 ISC3	16%	18%	17%	21%	24%
z114 1x IFB	13%	14%	14%	17%	19%
z114 12x IFB	12%	13%	12%	15%	17%
z114 12x IFB3	NA	NA	10%	12%	13%
z196 ISC3	16%	17%	17%	21%	24%
z196 1x IFB	13%	14%	13%	16%	18%
z196 12x IFB	11%	12%	11%	14%	15%
z196 12x IFB3	NA	NA	9%	11%	12%
zEnterprise EC12 ISC3	16%	17%	17%	21%	24%
zEnterprise EC12 1x IFB	13%	13%	13%	16%	18%
zEnterprise EC12 12x IFB	11%	11%	11%	13%	15%
zEnterprise EC12 12x IFB3	9%	9%	9%	10%	11%

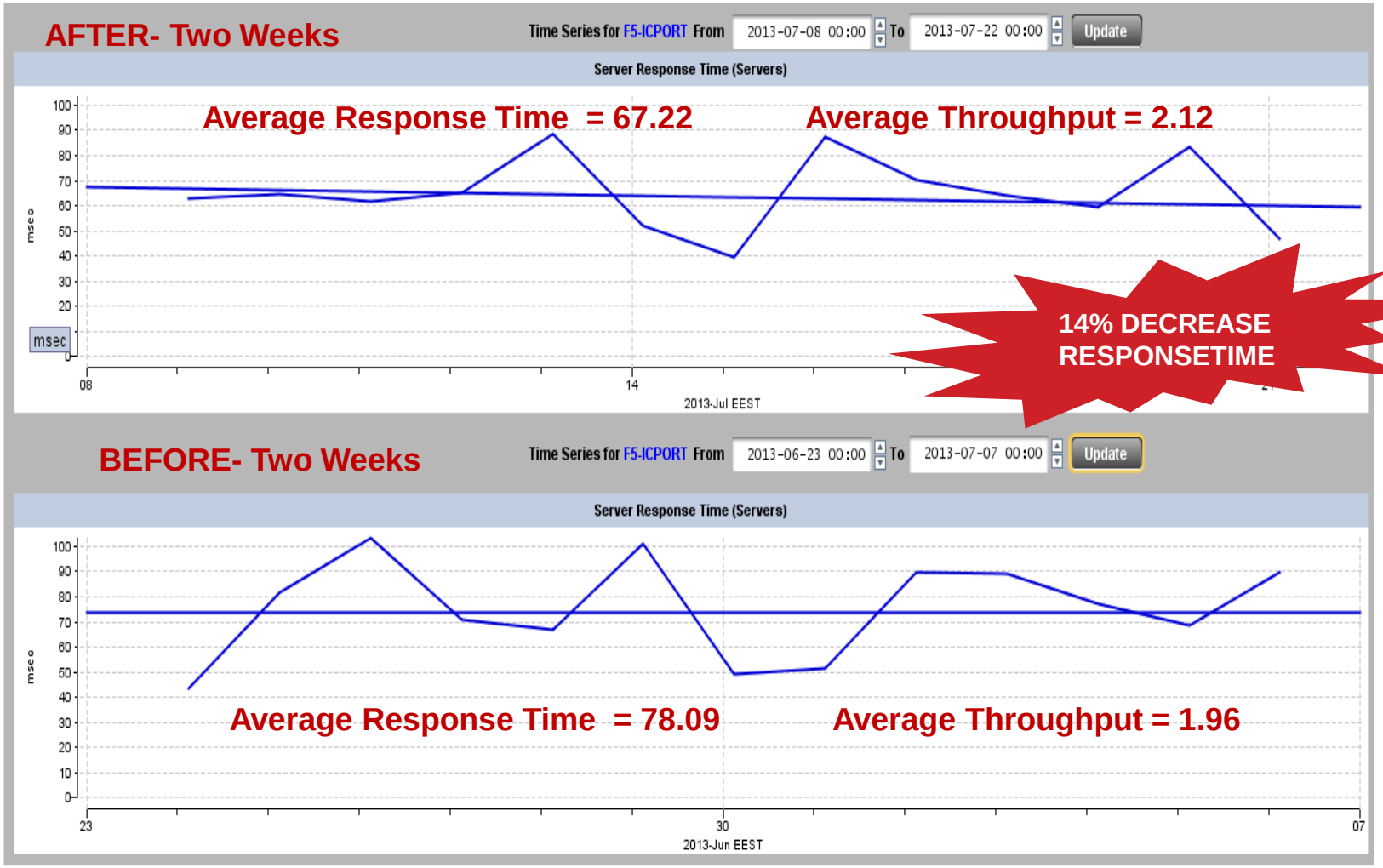
With z/OS 1.2 and above, synch->asynch conversion caps values in table at about 18%

IC links scale with speed of host technology and would provide an 8% effect in each case

How Are My End Users Effected ?
End User View

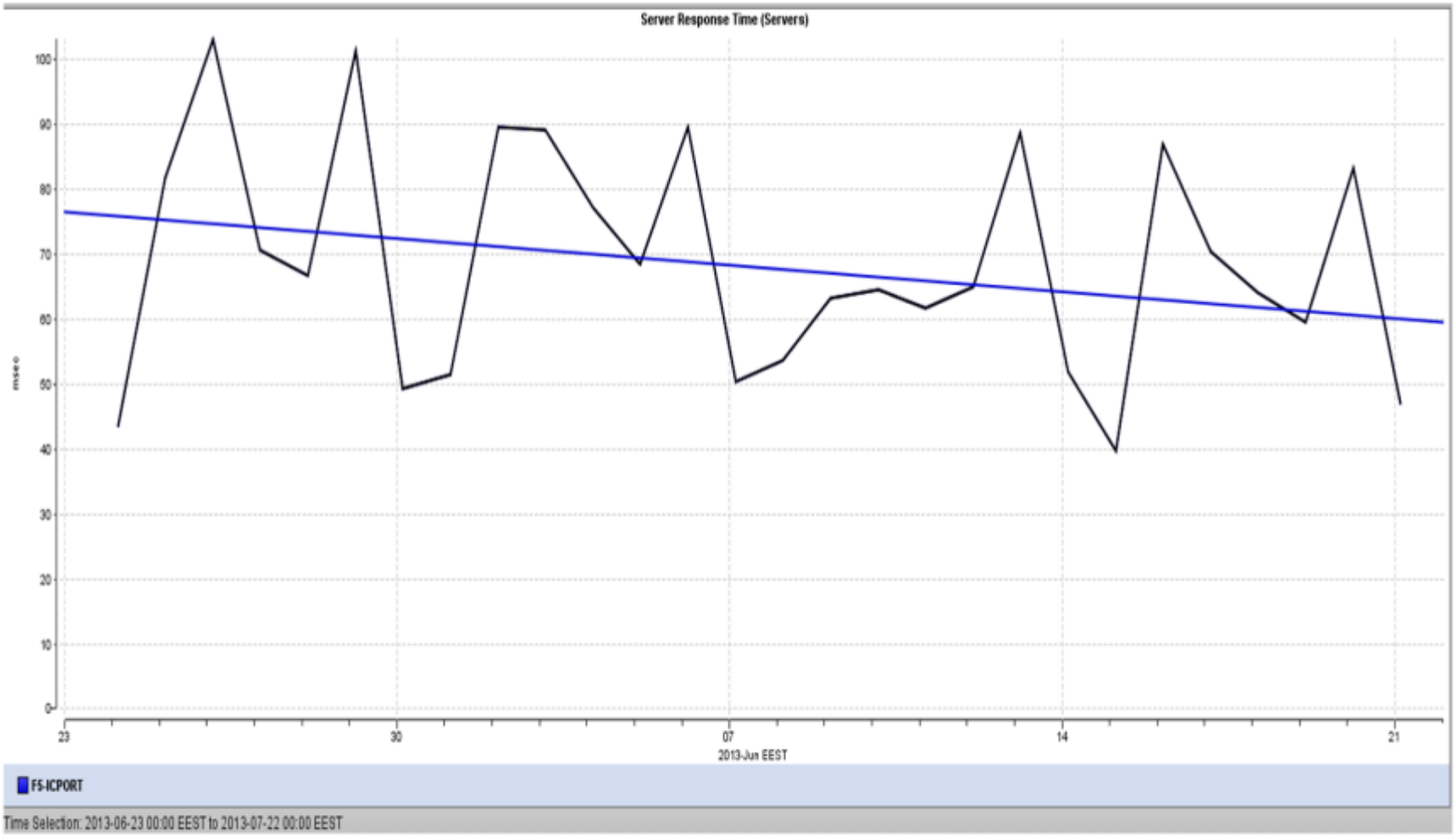
How Did Upgrade Effect End Users?

14 % DECREASE IN RESPONSETIME THAT IS SEEN FROM OUTSIDE OF MAINFRAME



How Did Upgrade Effect End Users?

TREND VIEW - RESPONSETIME

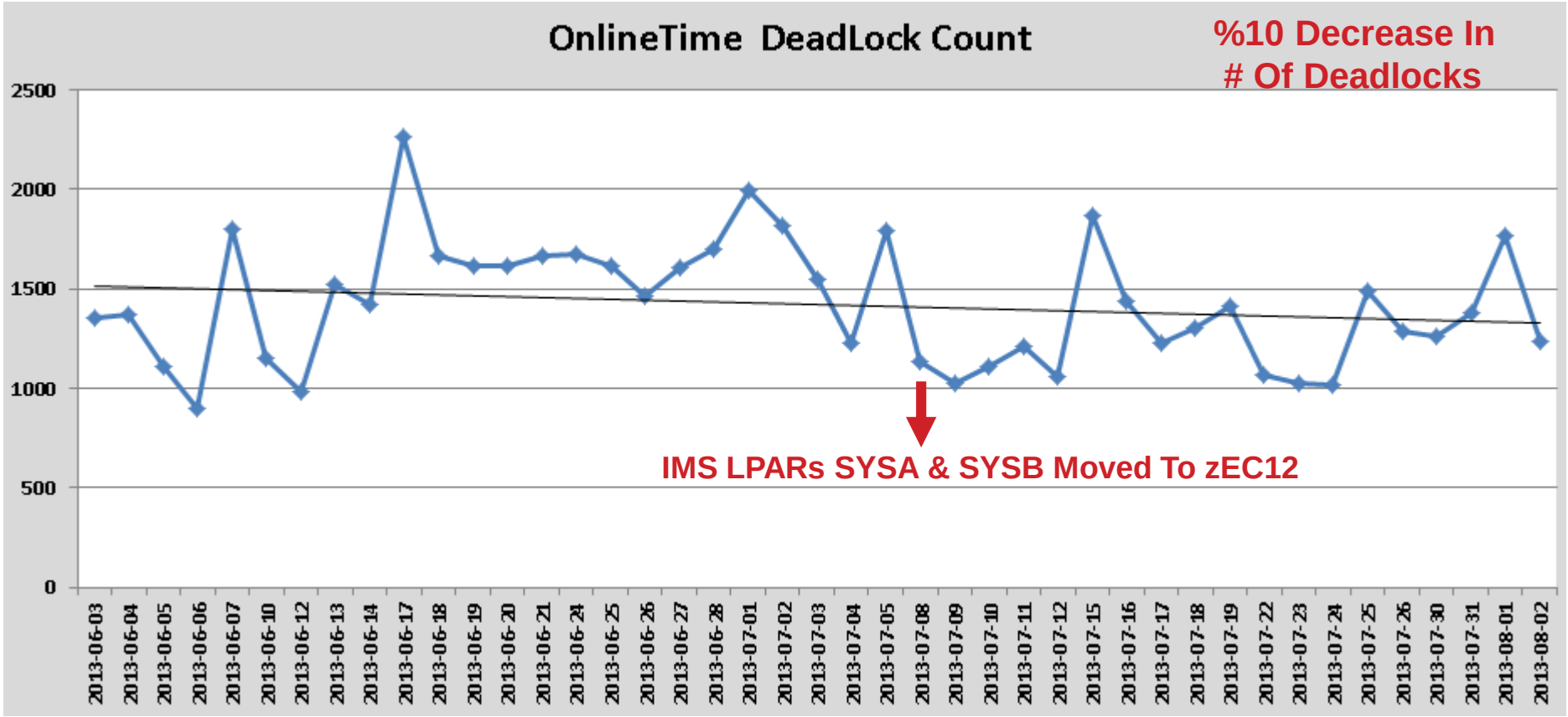


Side Effect ?

Are There Any Side Effects ?

Checking Side Effects

When We Checked 2 months of Data ,we realize that it is not a Side Effect! .
Just opposite = There is nearly 10 % Decrease In # Of IMS Deadlocks



Checking Side Effects

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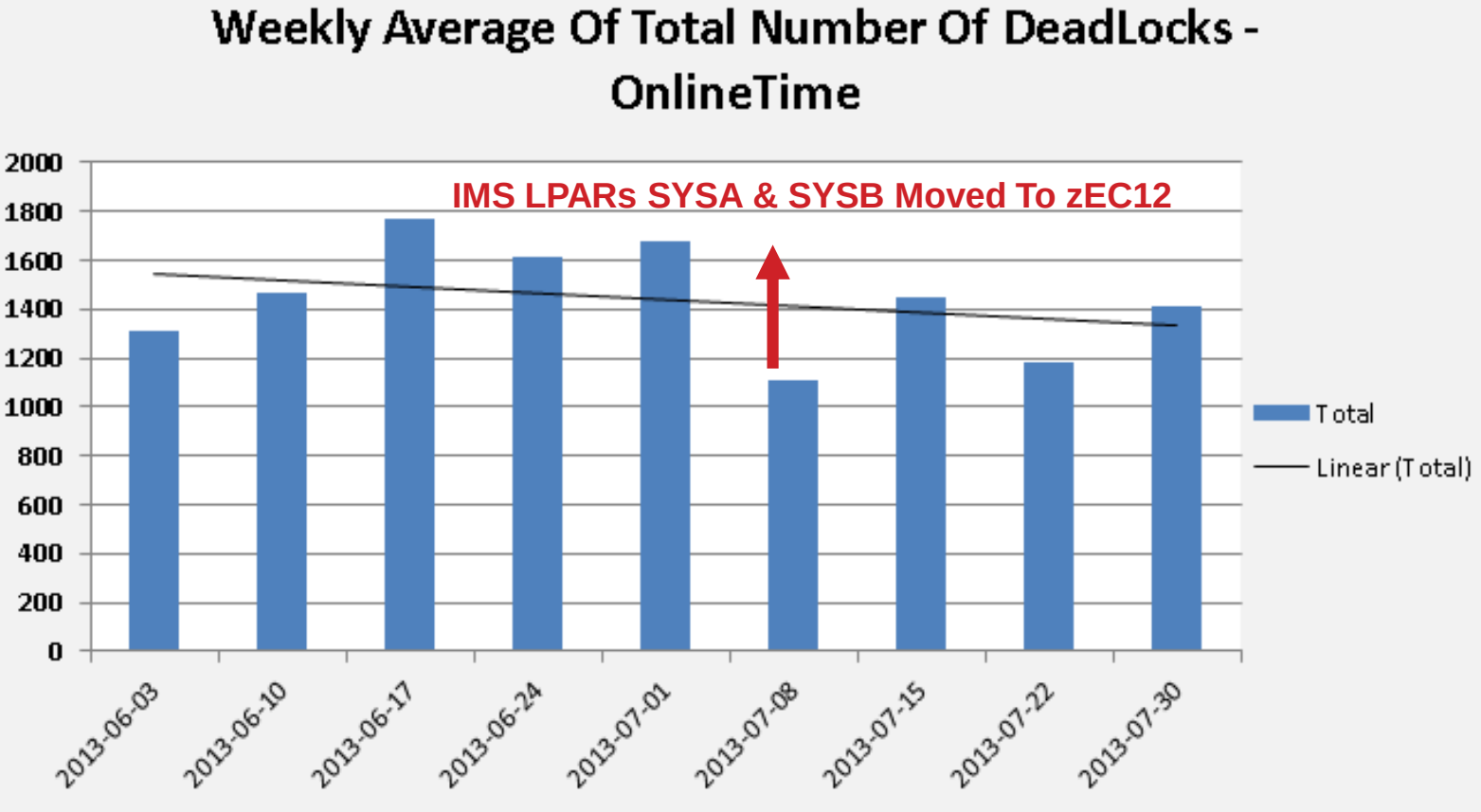
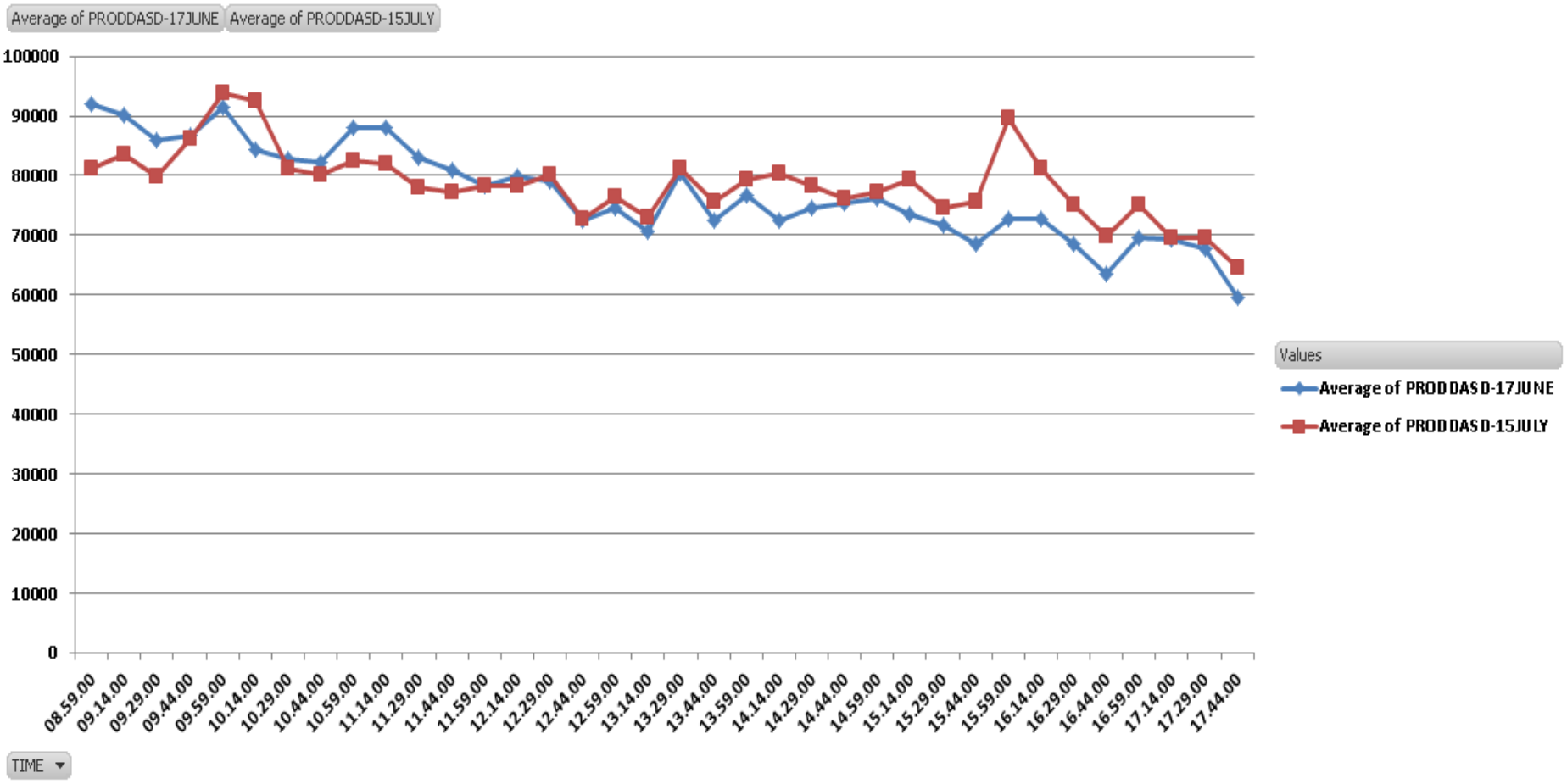


PEAK DAY COMPARISON
DASD I/O View
(Also Side Effect Check)

Production Total DASD RATE Online Time

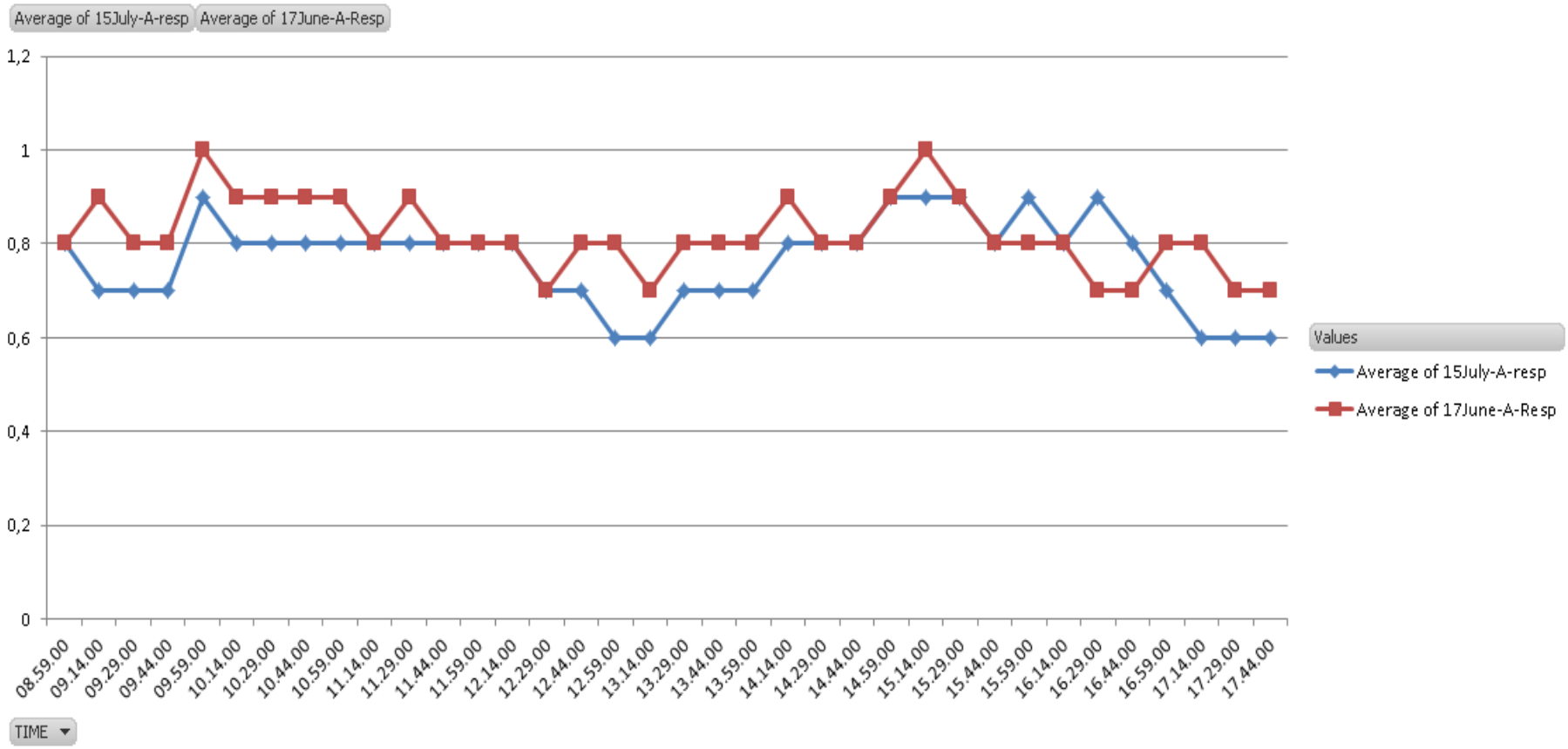
We were not high utilized in z10s,

So not that much increase in DASD Rate + Not cause any bottleneck



Production SYSA DASD ResponseTime (millisecs) Online Time

Started Using New I/O Response Time Component – zEC12 Feature I/O Interrupt Delay – (Not like other components)



Continuing Processes & Future Plans

Useful Links & More Information

For Sure SHARE Website

Great sessions in This SHARE as well as previous SHARE sessions – MVS Program

Resourcelink Website

https://www-304.ibm.com/servers/resourcelink/svc03100.nsf?Opendatabase

Exception Letter, CPU MF Counter document, PR/SM Planning, HMC & SE Users Guide and many more….

LSPR

https://www-304.ibm.com/servers/resourcelink/lib03060.nsf/pages/lsprindex?OpenDocument&pathID=

zPCR Download Website

http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/PRS1381?OpenDocument&TableRow=4.1.0#4.1.

IBM WSC Website - Techdocs

http://www-03.ibm.com/support/techdocs/atsmastr.nsf/Web/TechDocs

IBM WLM – LPAR DESIGN TOOL DOWNLOAD

http://www-03.ibm.com/systems/z/os/zos/features/wlm/tools/WLMsetupdesigntools.html

RMF User Guide – Chapter 15 Overview And Exception conditions

2011-SHARE –Anaheim Using and Getting Benefit From SMF113 Records :Customer Experience
2012-SHARE-Atlanta Migrating From z10 ICBs To z196 Infiniband –Detail Performance Study
2012-SHARE-Atlanta Analyzing/Monitoring/Measuring Memory Usage And Understanding z/OS Memory Management : Performance View

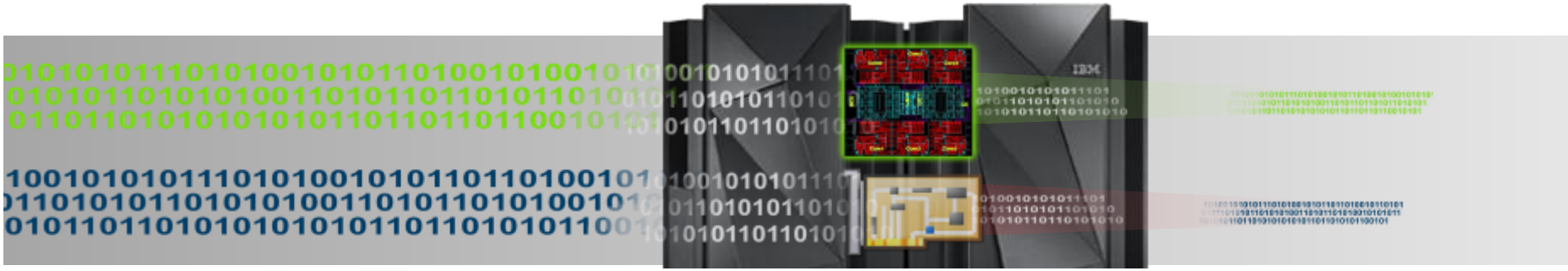
zEC12 GA2 And Other ENHANCEMENTS Thanks To Harv Emery – IBM WSC

New innovations available on zBC12 and zEC12

Data Compression Acceleration	High Speed Communication Fabric	Flash Technology Exploitation	Proactive Systems Health Analytics	Hybrid Computing Enhancements
Reduce CP consumption, free up storage & speed cross platform data exchange	Optimize server to server networking with reduced latency and lower CPU overhead	Improve availability and performance during critical workload transitions, now with dynamic reconfiguration; Coupling Facility exploitation (SOD)	Increase availability by detecting unusual application or system behaviors for faster problem resolution before they disrupt business	x86 blade resource optimization; New alert & notification for blade virtual servers; Latest x86 OS support; Expanding futures roadmap
zEDC Express	*10GbE RoCE Express*	*IBM Flash Express*	*IBM zAware*	*zBX Mod 003; zManager Automate; Ensemble Availability Manager; DataPower Virtual appliance SoD*

zEnterprise Data Compression (zEDC) - can help to reduce CPU and storage

Every day 2.5 quintillion bytes of data are created



Compress your data *4X** *(efficient system data compression)*

*Up to 118X reduction in CPU and up to 24X throughput improvement when zlib uses zEDC ***

Efficiently compress active data by providing a low CPU, high performance, dedicated compression accelerator

Industry standard compliance compression for cross platform data distribution **

Typical Client Use Cases:

Significant disk savings with trivial CPU cost for large BSAM/QSAM sequential files ***

More efficiently store audit data in application logs

Reduce the amount of data needed for data migration and backup/restore **

Transparent acceleration of Java compressed applications **

Data Ready

NEW **zEDC Express**

NEW **z/VM 6.3 support for guests*****

NEW **z/OS V2.1 zEDC**

* The amount of data sent to an SMF logstream can be reduced by up to 75% using zEDC compression – reducing logger overhead

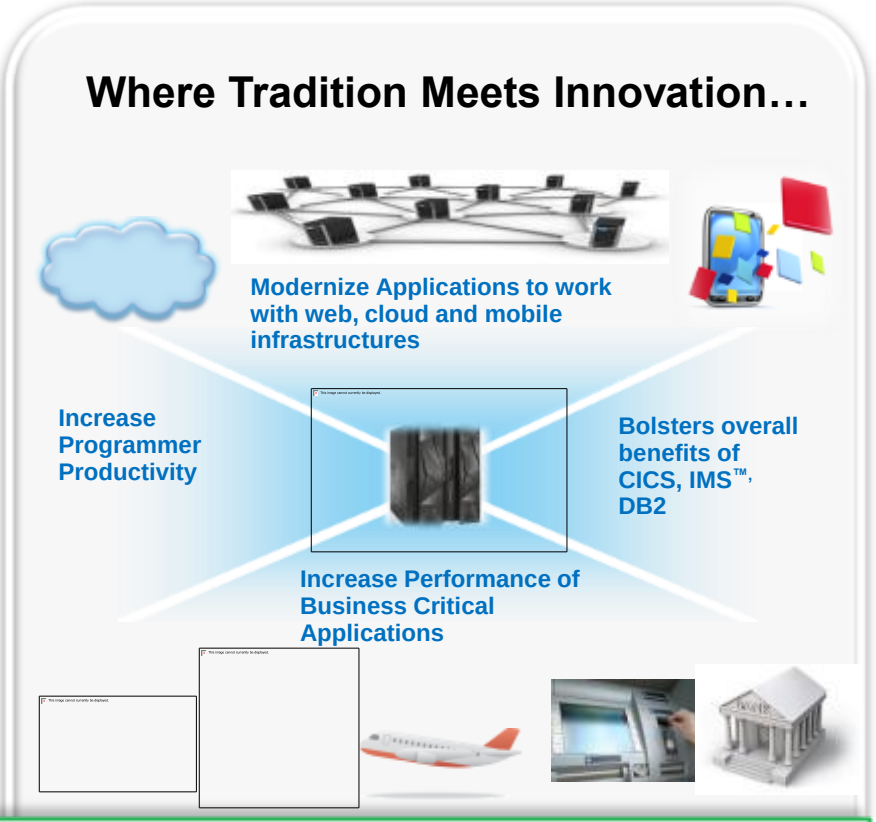
** These results are based on projections and measurements completed in a controlled environment. Results may vary by customer based on individual workload, configuration and software levels

*** All statements regarding IBM's future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only.

Enterprise COBOL for z/OS v5.1

The key to supercharging IBM System z Applications

- **Advanced technology designed to optimize COBOL programs and fully exploit System z hardware**
  - Delivers greater than 10% performance improvement over Enterprise COBOL v4 for well structured, CPU-intensive batch applications on System z[1]
  - Many numerically intensive programs have shown performance increases greater than 20%[1]
  - Maintains compatibility with previous COBOL releases
- **New programming and application modernization capabilities.**
  - Enables users to deliver enhancements to business critical applications quicker with less cost and lower risk
- **Allows users, who implement sub-capacity tracking, to reduce administrative overhead**
- **Supports the ecosystem of COBOL development tools supplied by IBM and ISVs.**



CUSTOMER VALUE

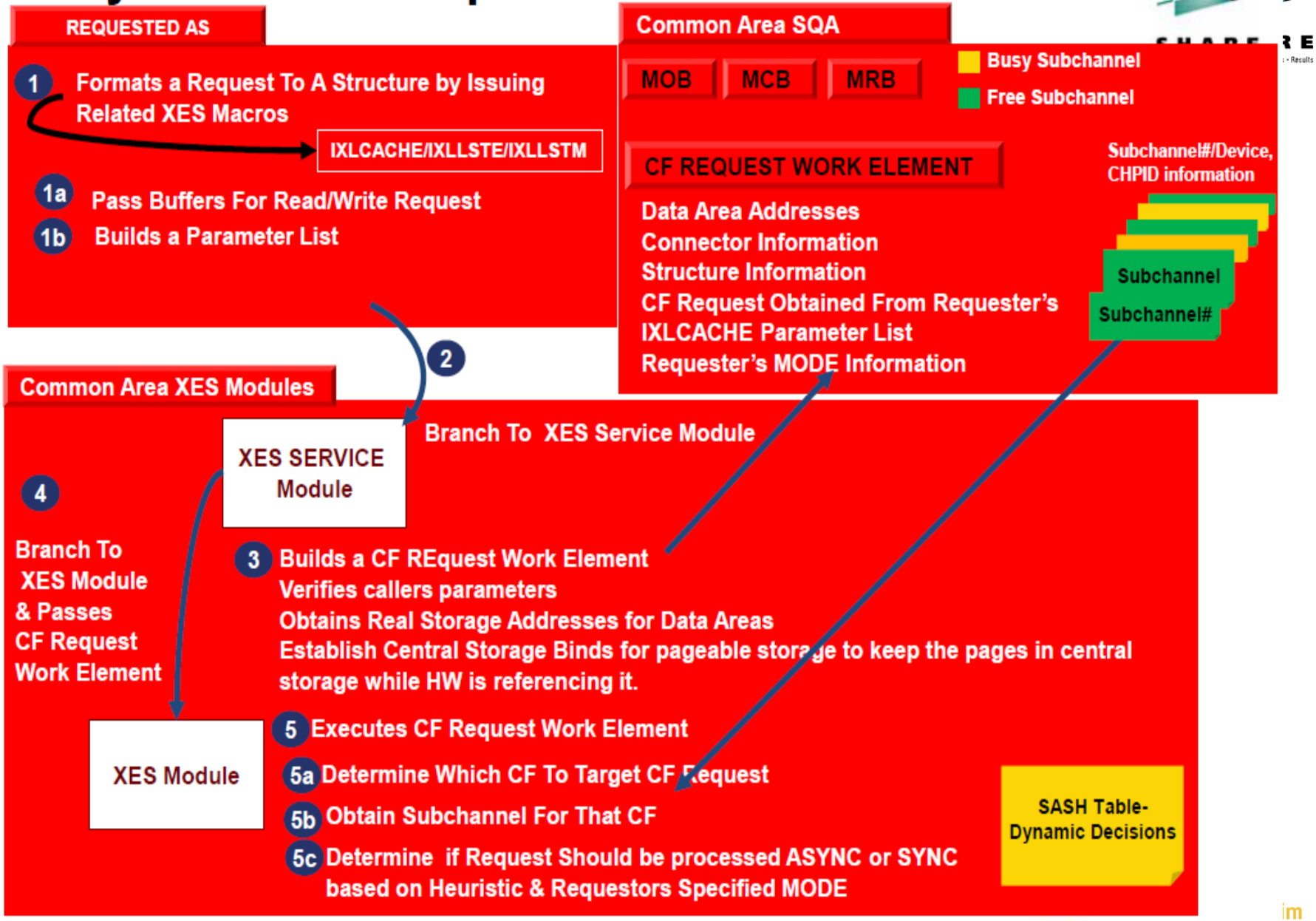
[1] Results are based on an internal compute-intensive test suite. Performance results from other applications may vary.

SPECIAL THANKS TO ….

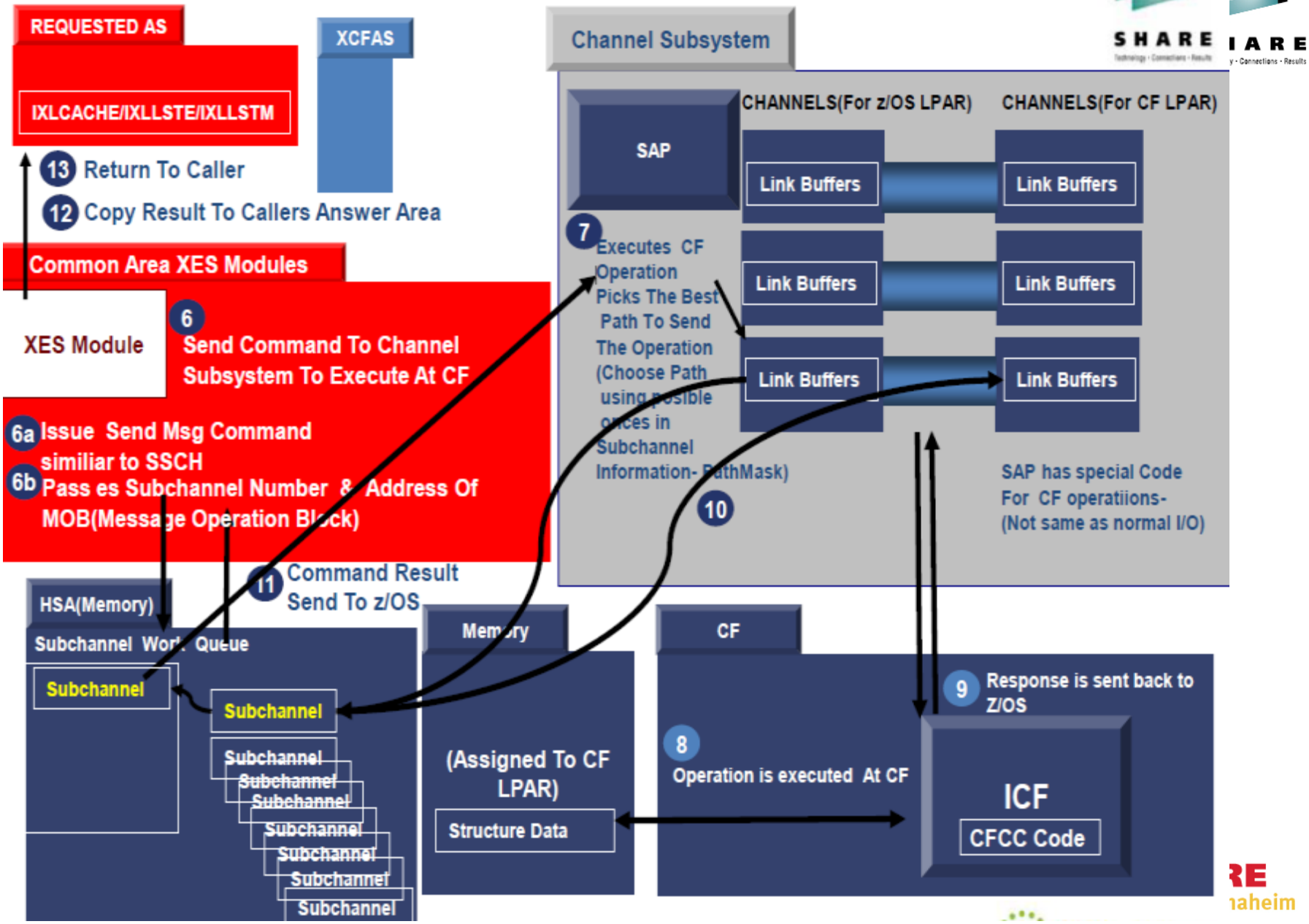
GARY KING - IBM Performance
JOHN BURG – IBM WSC
GEORGETTE KURT – IBM Parallel Sysplex
HORST SINRAM – IBM WLM
HARV EMERY – IBM WSC

Backup Slides

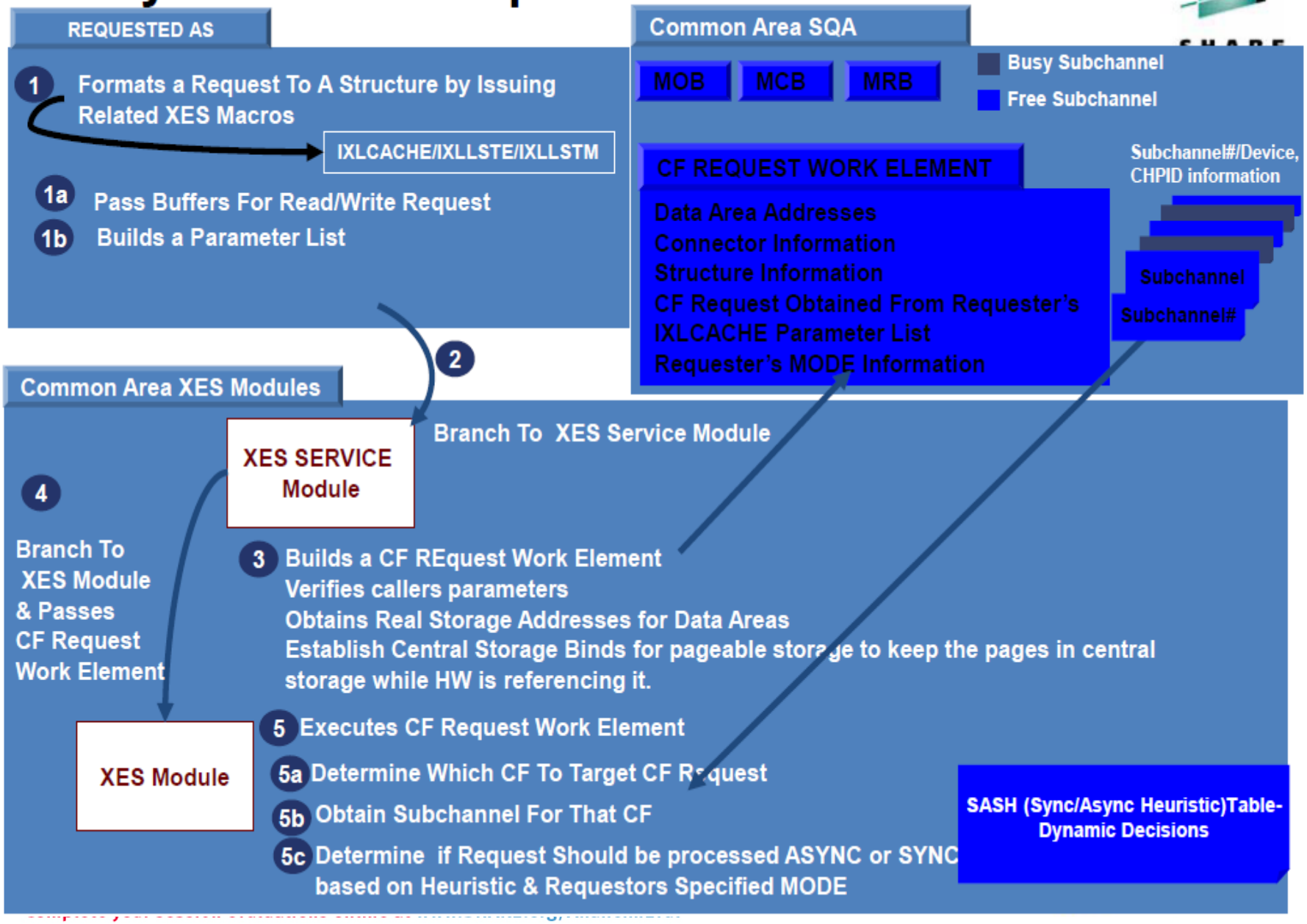
CF Syncronous Request Flow-1



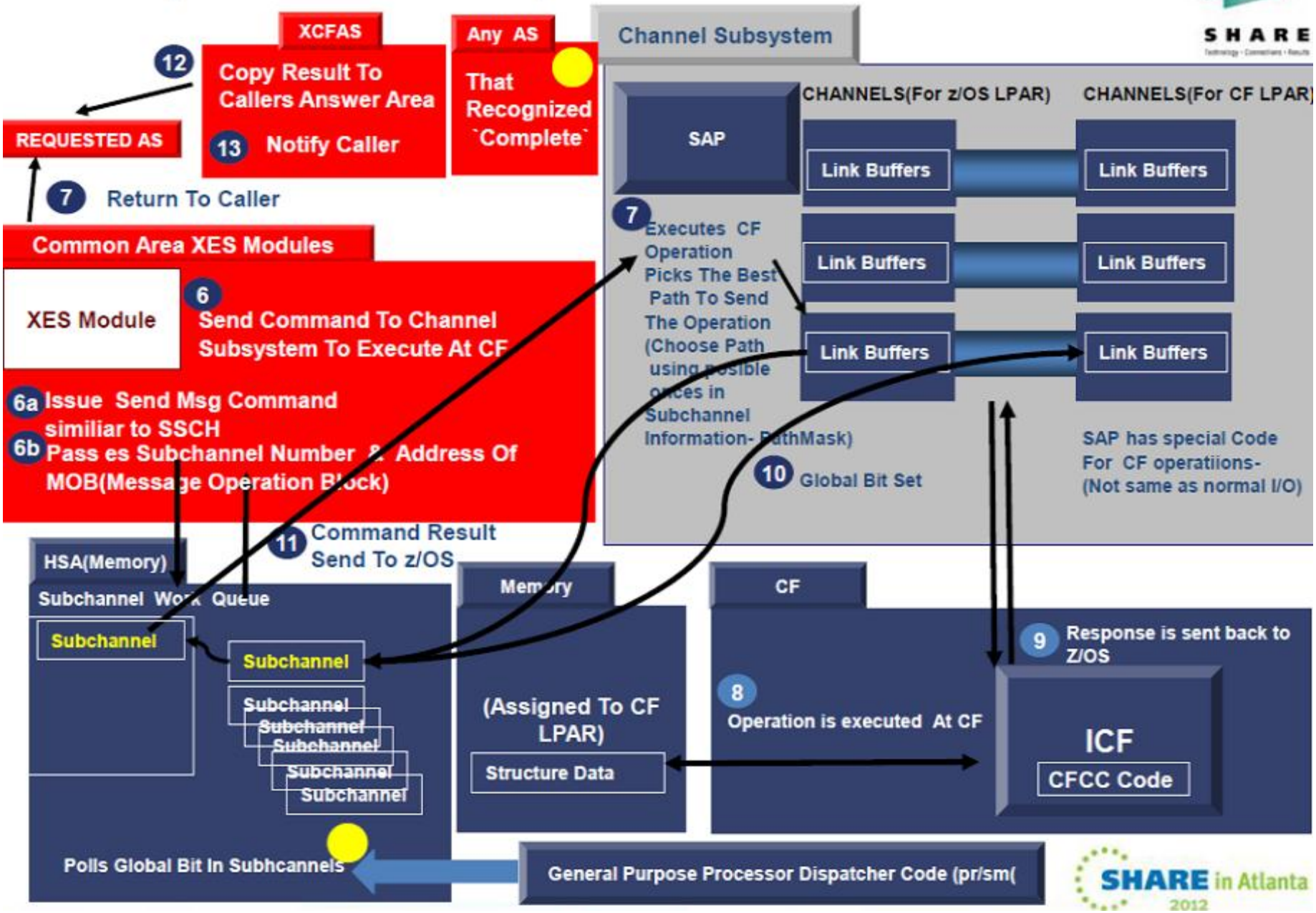
CF Syncronous Request Flow-2



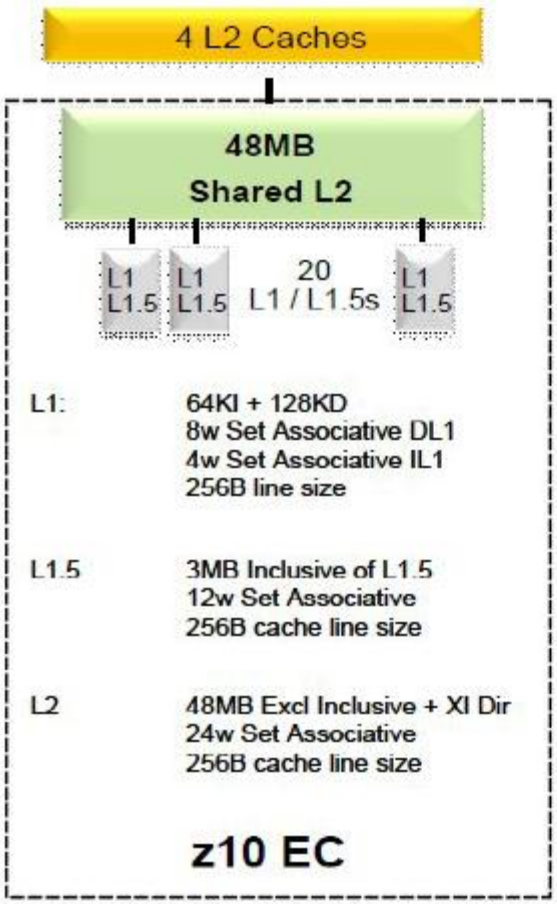
CF Asyncronous Request Flow -1

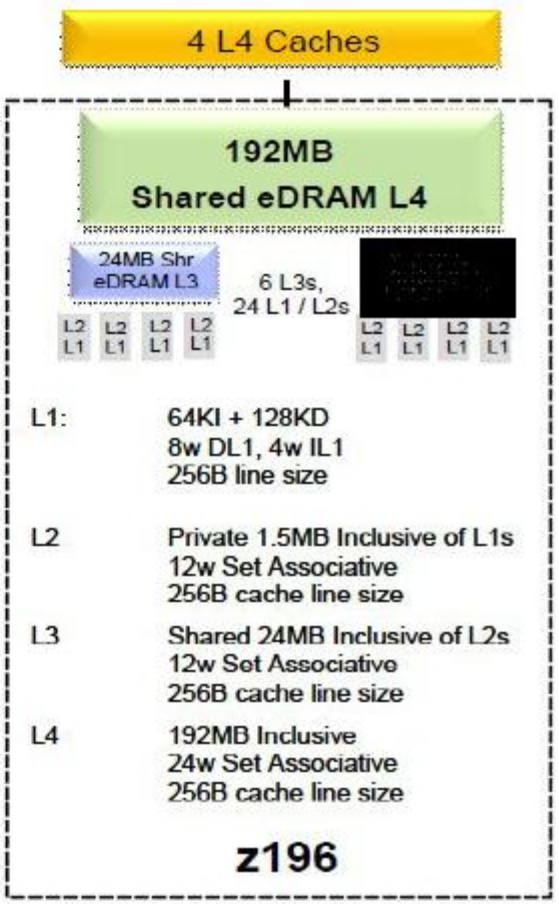


CF Asyncronous Request Flow -2



Backup Slide z10 – z196 Differences





Backup Slide z196 – zEC12 Differences

z196 EC MCM vs zEC12 MCM Comparison

z196 MCM

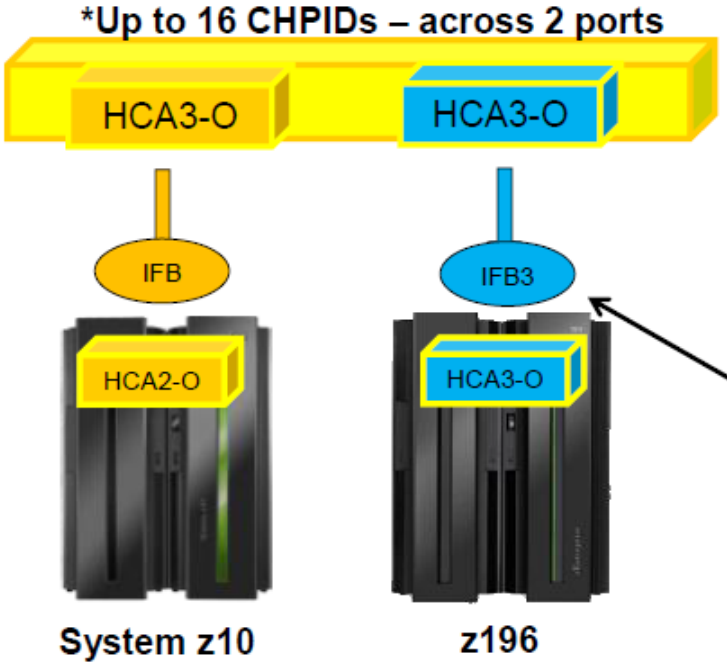
- **MCM**
  - –96mm x 96mm in size
  - –6 PU chips per MCM
    - Quad core chips with 3 or 4 active cores
    - PU Chip size 23.7 mm x 21.5 mm
    - 5.2 GHz
    - Superscalar, OoO execution
    - L1: 64 KB I / 128 KB D private/core
    - L2: 1.5 MB I+D private/core
    - L3: 24 MB/chip – shared
  - –2 SC chips per MCM
    - L4: 2 x 96 MB = 192 MB L4 per book
    - SC Chip size 24.5 mm x 20.5 mm
  - –1800 Watts

zEC12 MCM

- **MCM**
  - –96mm x 96mm in size
  - –6 PU chips per MCM
    - Hex-core chips with 4 to 6 active cores
    - PU Chip size 23.7 mm x 25.2 mm
    - 5.5 GHz
    - Improved superscalar and OoO execution
    - L1: 64 KB I / 96 KB D private/core
    - L2: 1 MB I / 1 MB D private/core
    - L3: 48 MB/chip - shared
  - –2 SC chips per MCM
    - L4: 2 x 192 MB = 384 MB L4 per book
    - SC Chip size 26.72 mm x 19.67 mm
  - –1800 Watts

New PSIFB Protocol & Infiniband Fanout Cards

New 12x InfiniBand fanout cards, exclusive to z196 and z114



Attachment to System z9 HCA1 not supported

Two protocols (IFB & IFB3)

1. 12x IFB = HCA3-O to HCA2-O
2. 12x IFB3 = HCA3-O to HCA3-O (see below)

- **Improved service times, 12x IFB3 service times are designed to be 40% faster than 12x IFB**

12x IFB3 protocol activation requirements

– Maximum of **four** CHPIDs per HCA3-O port

- **If more than four CHIPDs are defined per port, links will run at normal 12x IFB service times**
- **IFB3 protocol activated as long as 4 CHPIDs or less are defined. No configuration settings required.**
- Performance considerations may reduce the number of CHPIDs per port

Note: The InfiniBand link data rates of 6 GBps, 3 GBps, 2.5 Gbps, or 5 Gbps do not represent the performance of the link. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.