

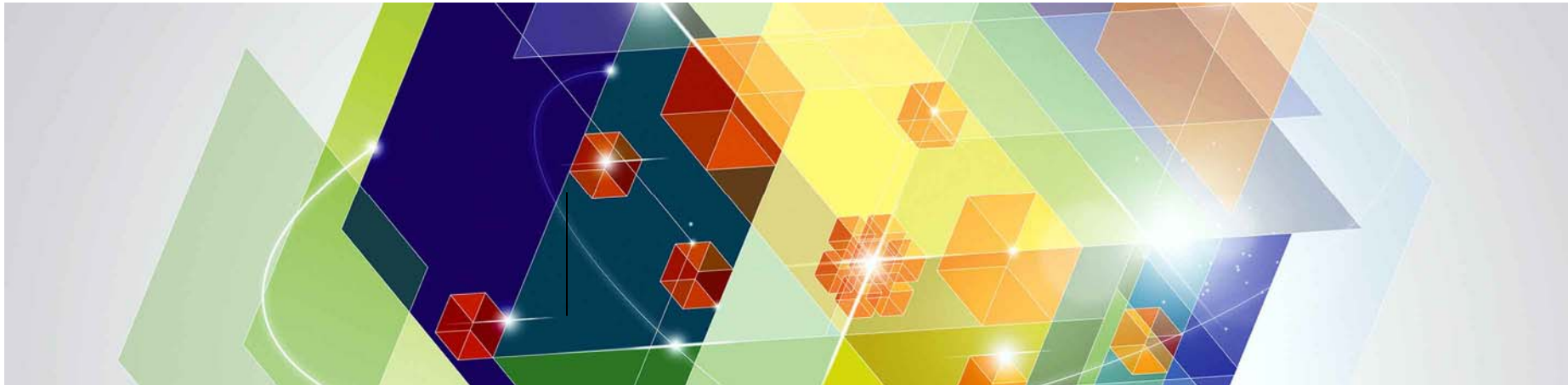
# IBM z196 and z114 Hardware Overview and Update

Session ID: 10606

Speaker: Harv Emery



System z – Freedom Through Design



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## Introducing the next steps in the evolution of zEnterprise



**NEW**

- **Innovations to improve zEnterprise at its core**
  - New I/O Infrastructure and function ([Session 10617](#))
- **Increased flexibility to deploy and manage enterprise clouds**
- **A new zEnterprise designed for mid-sized clients**



# zEnterprise System Structure

## IBM zEnterprise Unified Resource Manager

IBM zEnterprise 196 (z196™)



OR

IBM zEnterprise 114 (z114™)



AND  
Optionally



IBM zEnterprise BladeCenter® Extension (zBX™)

System z – Freedom Through Design

## New Options: More System x Blades, larger memory and new options for SAN and Network Connectivity

- **System x Blades in the zBX**
  - Select IBM BladeCenter HX5 7873 dual-socket 16-core blades
  - **Four** memory choices: 64, 128, **192 and 256 GB**
  - Ordered and fulfilled through System x providers and installed into the zBX by the customer
  - The zBX web page will host current blade ordering information: [http://www.ibm.com/common/ssi/cgi-bin/ssialias?infotype=SA&subtype=WH&appname=STGE\\_ZS\\_ZS\\_USEN&htmlfid=ZSL03128USEN&attachment=ZSL03128USEN.PDF](http://www.ibm.com/common/ssi/cgi-bin/ssialias?infotype=SA&subtype=WH&appname=STGE_ZS_ZS_USEN&htmlfid=ZSL03128USEN&attachment=ZSL03128USEN.PDF)
  - Blades assume System z warranty and maintenance when installed in the zBX
- **Available SAN connections per BladeCenter chassis**
  - Increased from 4 to 12 FCS 8 Gbps SX links to SAN directors
  - All links active with load balancing at blade login
  - Shared by POWER7 and System x blades in the chassis
- **Both 1 Gbps and 10 Gbps network connection options**
  - **1 Gbps fibre optic SX or LX to customer routers and servers**
  - 10 Gbps LR or SR to customer routers and servers or for IEDN connections zBX to zBX or zBX to zEnterprise OSX channels

**NOTE: The IBM DB2 Analytics Accelerator for z/OS (IDAA) can be connected to the zBX at 10 Gbps as a supported customer network server.**

### *IBM zEnterprise BladeCenter Extension (zBX) Machine Type: 2458 Mod 002*

#### **Optimizer:**

- IBM WebSphere DataPower Integration Appliance XI50z for zEnterprise

#### **Select IBM Blades:**

- IBM BladeCenter PS701 Express
- IBM BladeCenter HX5 7873

One to four – 42u racks – capacity for up to 112 blades

Configured for high availability

No MIPS/MSUs rating

- Up to 112 PS701 Power blades
- **Up to 56<sup>1</sup> HX5 System x blades (March 30, 2012)**
- Up to 28 DataPower XI50z blades (double-wide)



*... managed by the  
zEnterprise Unified Resource Manager*

*<sup>1</sup> All statements regarding IBM future direction and intent are subject to change or withdrawal without notice, and represents goals and objectives only.*

## Extending zEnterprise Unified Resource Manager *Continuing to add function and management*



- **Operational Controls enhanced with auto-discovery and configuration support for new resources (December 16, 2011)**
  - ▶ Dynamic discovery and configuration of storage resources by Unified Resource Manager
- **Extending management functions of Unified Resource Manager with programmatic access (December 16, 2011)**
  - ▶ Unified Resource Manager APIs enable discovery, monitoring and management of ensemble resources using external tools
    - Open documented interface available for clients
      - Access using common scripting languages like Perl and Python
    - IBM Tivoli® will be taking advantage of the APIs<sup>1</sup>:
      - **SOD**: IBM intends to enhance the Tivoli Integrated Service Management for System z portfolio to take advantage of the additional zEnterprise ensemble monitoring and management information provided by the Unified Resource Manager APIs.
    - CA Technologies, Dovetailed Technologies, CSL International and other ISVs are interested in taking advantage of the APIs



### ▪ **Management Enhancements (March 6, 2012)**

- ▶ **Server Application State Protocol (SASP) Load Balancing**
- ▶ **Support for SAP running on Linux on System x or Windows on System x blades in a zBX**
- ▶ **HiperSockets Integration with the IEDN<sup>2</sup>**
- ▶ **Support for Improved Network Monitoring and Metrics<sup>2</sup>**

1. All statements regarding IBM future direction and intent are subject to change or withdrawal without notice, and represents goals and objectives only.

2. Available March 6, 2012 except z/VM 6.2 support which is planned for April 13, 2012

## Hardware Withdrawals: IBM System z10 EC and IBM System z10 BC

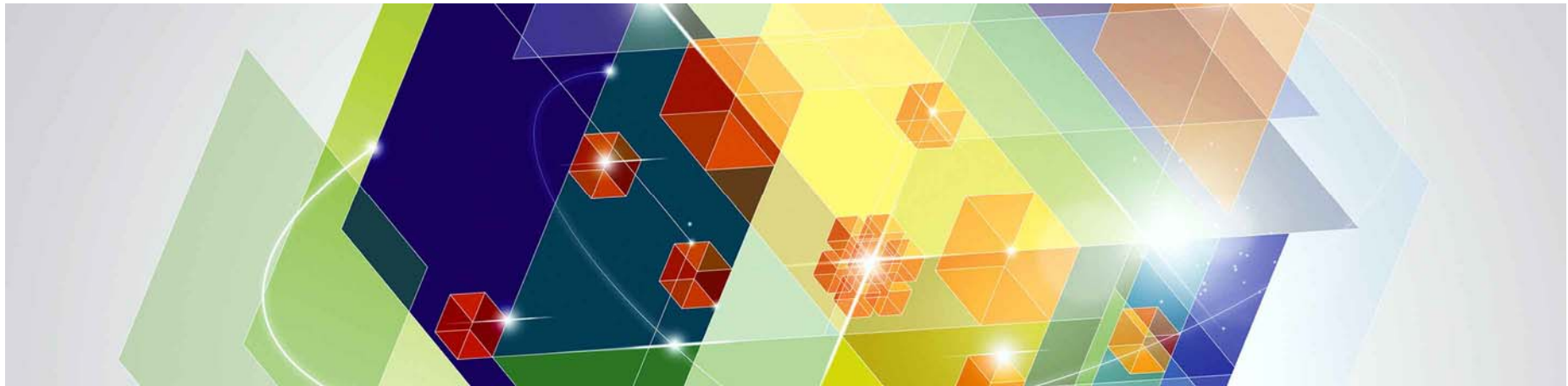
- **Effective June 30, 2012, IBM is withdrawing the following selected products from marketing**
  - All models of the IBM System z10 Enterprise Class (z10 EC) and all upgrades to the z10 EC from the IBM eServer zSeries 990 (z990), IBM System z9 EC (z9 EC), or IBM System z10 BC (z10 BC).
  - All models of the IBM System z10 Business Class (z10 BC) and all upgrades to the z10 BC from the IBM eServer zSeries 890 (z890) or IBM System z9 BC (z9 BC).
  - Model conversions and hardware MES features applied to an existing z10 EC or z10 BC server.
- **Field installed features and conversions that are delivered solely through a modification to the machine's Licensed Internal Code (LIC) will continue to be available until June 30, 2013. After June 30, 2013, features and conversions that are delivered solely through a modification to the LIC will be withdrawn.**
- **The Capacity on Demand offerings that are configured prior to withdrawal are usable until the offering expiration date or termination date, as applicable**

## IBM zEnterprise 196 Feature

- **Effective December 31, 2011 IBM System z will withdraw from marketing the following feature on IBM zEnterprise 196 (z196):**
  - HCA2-O LR fanout for 1x IFB (#0168)
  - On or after the effective dates for the withdrawal of these offerings, you can no longer order these products directly from IBM.

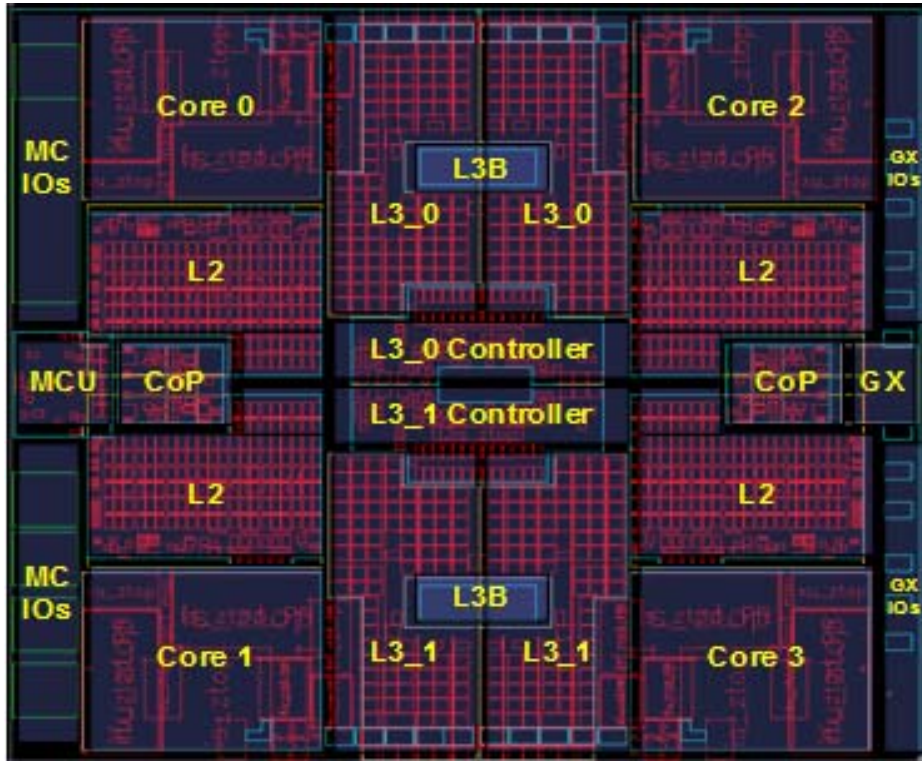
# zEnterprise Processors

System z – Freedom Through Design





## zEnterprise Quad Core PU Chip Detail



- **12S0 45nm SOI Technology**
  - 13 layers of metal
  - 3.5 km wire
- **1.4 Billion Transistors**

- **Chip Area – 512.3mm<sup>2</sup>**
  - 23.5mm x 21.8mm
  - 8093 Power C4's
  - 1134 signal C4's

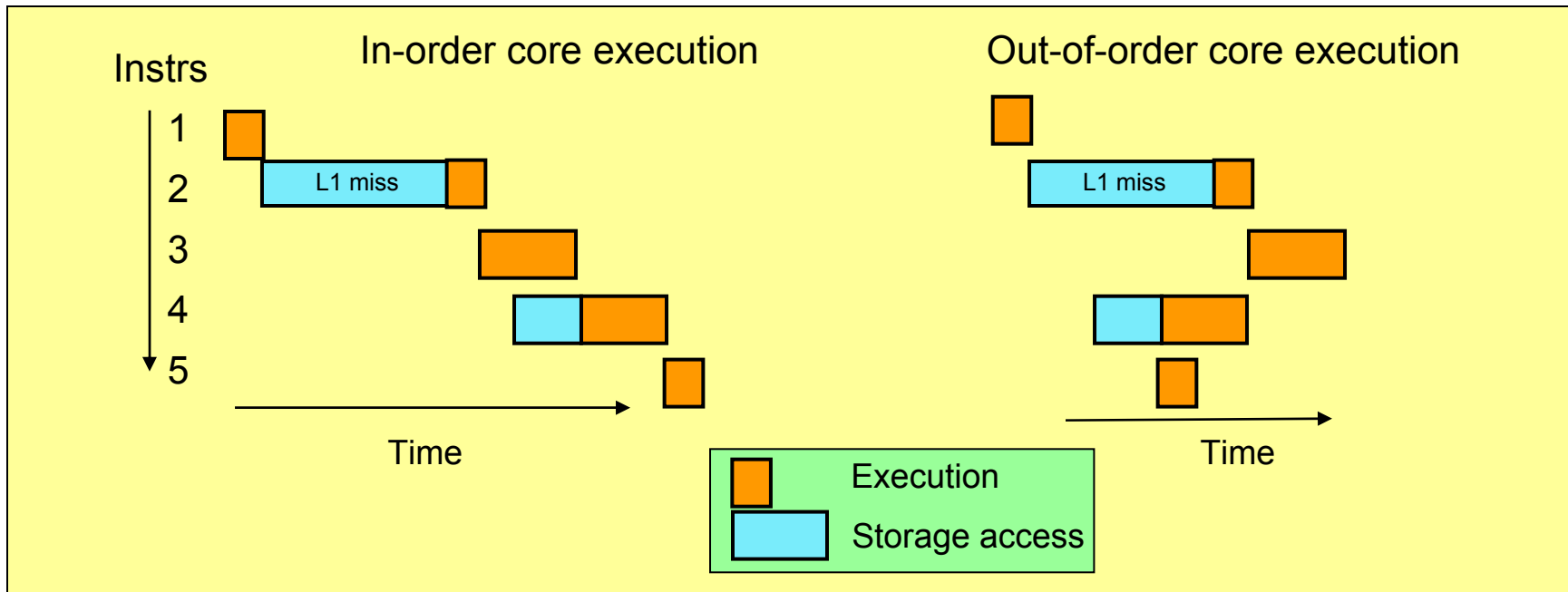
- **Three or four active cores per chip**
  - 5.2 GHz in z196
  - 3.8 GHz in z114
  - L1 cache/ core
    - 64 KB I-cache
    - 128 KB D-cache
  - 1.5 MB private L2 cache/ core
- **Two Crypto & compression accelerators**
  - Includes 16KB cache
  - Shared by two cores
- **eDRAM L3 Cache**
  - Shared by all four cores
  - 24 MB usable in z196
  - 12 MB usable in z114
- **Interface to SC chip / L4 cache**
  - 41.6 GB/sec to Storage Control (SC) chips
  - Two SCs in z196 multichip module (MCM)
  - One SC in a z114 CPC drawer
- **Memory Controller (MC)**
  - Interface to controller on memory DIMMs
  - Supports RAIM design

## New instructions and instruction enhancements Designed to provide new function and improve performance

- **High-Word Facility** (30 new instructions)
  - Independent addressing to high word of 64 bit General Purpose Registers
  - Effectively provides software with 16 additional registers for arithmetic
- **Interlocked-Access Facility** (12 new instructions)
  - Interlocked (atomic) load, value update and store operation in a single instruction
- **Load/Store-on-Condition Facility** (6 new instructions)
  - Load or store conditionally executed based on condition code
  - Dramatic improvement in certain codes with highly unpredictable branches
- **Distinct-Operands Facility** (22 new instructions)
  - Independent specification of result register (different than either source register)
  - Reduces register value copying
- **Population-Count Facility** (1 new instruction)
  - Hardware implementation of bit counting ~5x faster than prior software implementations
- **Floating-Point-Extension Facility** (21 new instructions, 34 instruction enhancements)
- **Message-Security Assist Extensions 3 and 4** – (5 new instructions, 6 instruction enhancements)
- **And more .....**

## zEnterprise Out-of-Order (OOO) Value

- **zEnterprise has the first System z CMOS out-of-order core**
- **This is the first System z out-of-order core since 1991**
- **OOO yields significant performance benefit for applications through**
  - Re-ordering instruction execution
    - Later (younger) instructions can execute ahead of an older stalled instruction
  - Re-ordering storage accesses and parallel storage accesses
- **OOO maintains good performance growth for traditional apps**



## z114 SCM Vs z196 MCM Comparison – Same PU and SC Chip

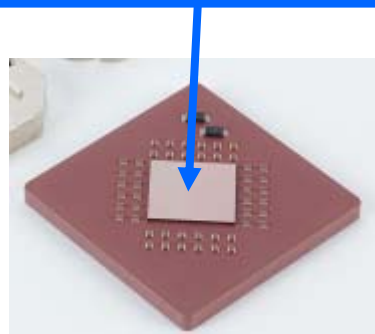
### z114 SCMs

- **PU SCM**
  - 50mm x 50mm in size – fully assembled
  - Quad core chip with 3 and 4 active cores
  - 2 PU SCMs for M05 and 4 PU SCMS for M10
  - PU Chip size 23.498 mm x 21.797 mm
- **SC SCM**
  - 61mm x 61mm in size – fully assembled
  - 1 SC SCM for M05, 2 SC SCMs for M10
  - 96 MB L4 cache per chip
  - SC Chip size 24.427 mm x 19.604 mm

**Single PU Chip  
without heatsink**

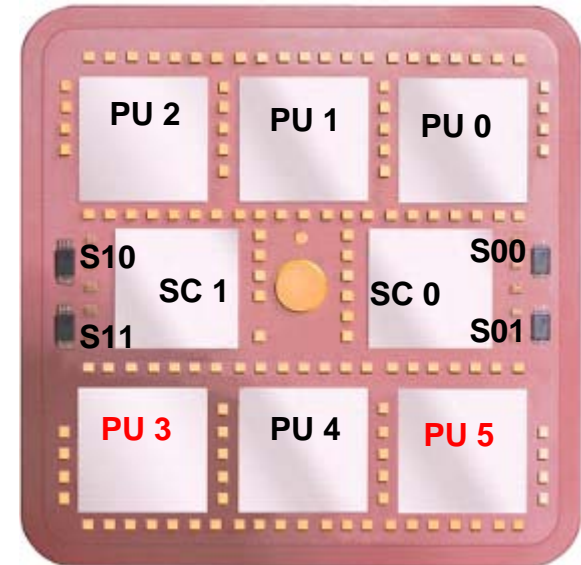


**Single SC Chip  
without heatsink**

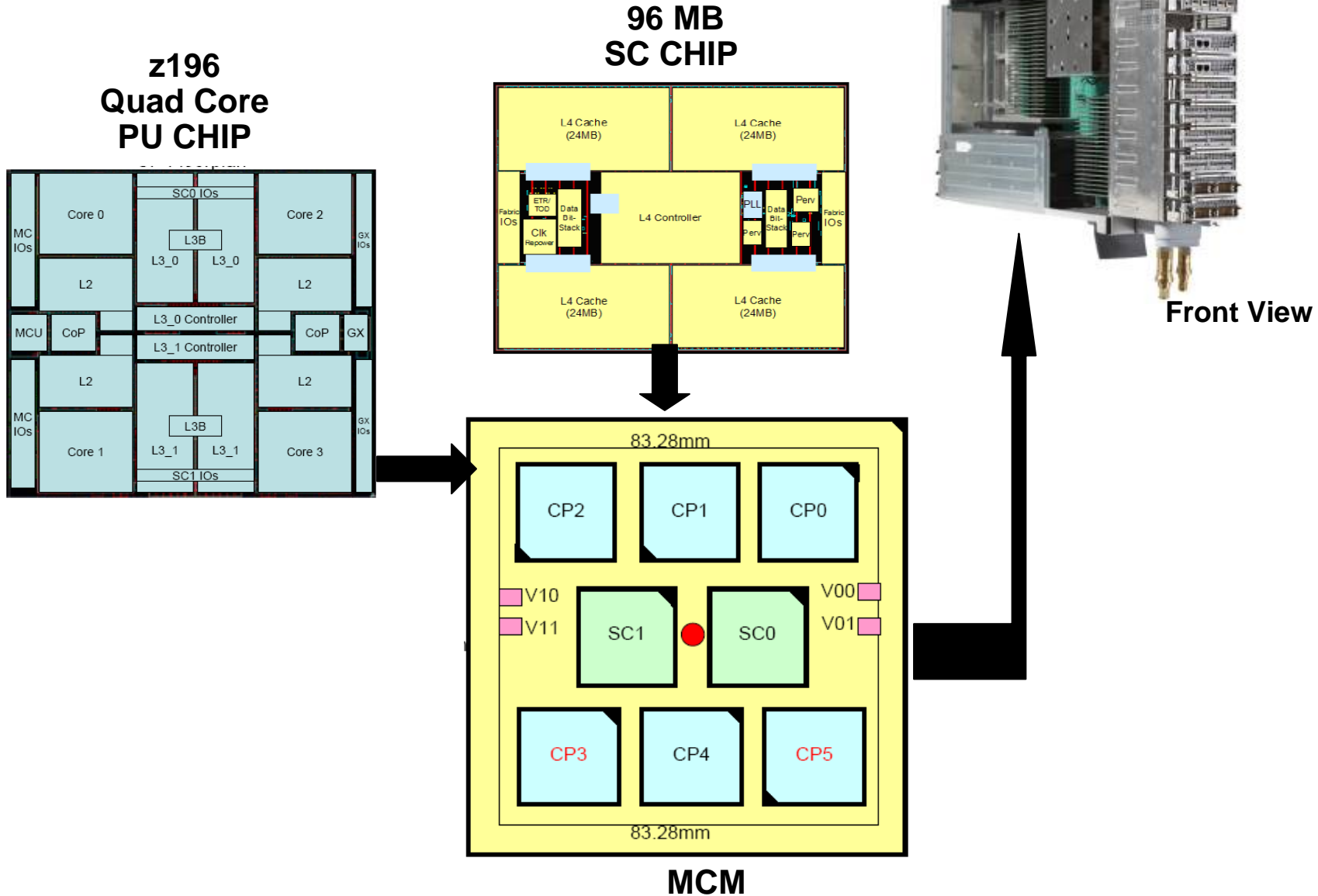


### z196 Multi Chip Module (MCM)

- **MCM**
  - 96mm x 96mm in size
  - 6 PU chips per MCM
    - Quad core chips with 3 or 4 active cores
    - PU Chip size 23.498 mm x 21.797 mm
  - 2 SC chips per MCM
    - 96 MB L4 cache per chip
    - SC Chip size 24.427 mm x 19.604 mm
  - Up to 4 MCMs for System



## z196 PU chip, SC chip and MCM



## z10 EC MCM vs z196 MCM Comparison

### z10 EC MCM

#### ▪ MCM

- 96mm x 96mm in size
- 5 PU chips per MCM
  - Quad core chips with 3 or 4 active cores
  - PU Chip size 21.97 mm x 21.17 mm
  - 4.4 GHz
  - Superscalar, In order execution
  - L1: 64K I / 128K D private/core
  - L1.5: 3M I+D private/core
- 2 SC chips per MCM
  - L2: 2 x 24 M = 48 M L2 per book
  - SC Chip size 21.11 mm x 21.71 mm

–1800 Watts

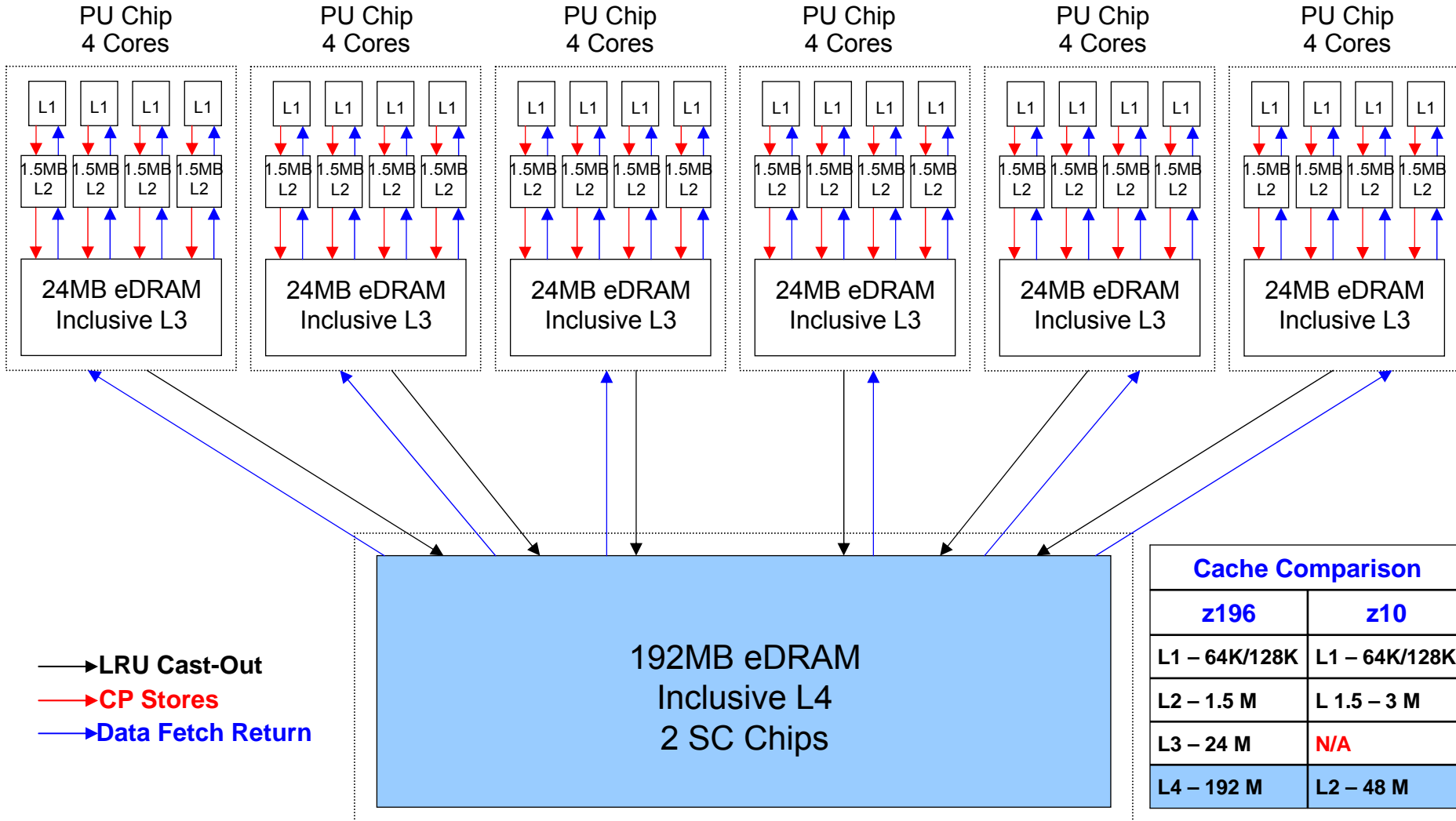
### z196 MCM

#### ▪ MCM

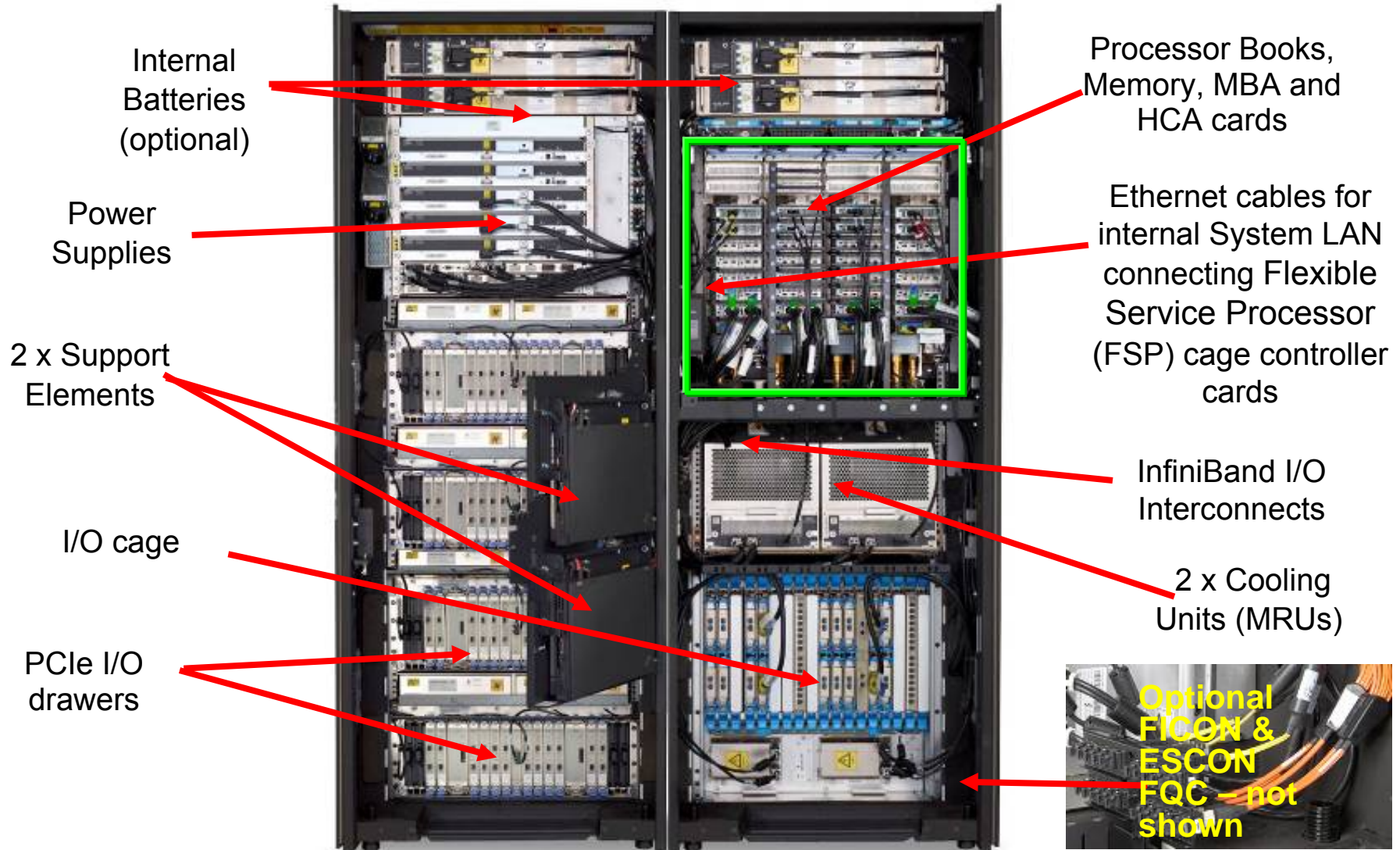
- 96mm x 96mm in size
- 6 PU chips per MCM
  - Quad core chips with 3 or 4 active cores
  - PU Chip size 23.7 mm x 21.5 mm
  - 5.2 GHz
  - Superscalar, OOO execution
  - L1: 64K I / 128K D private/core
  - L2: 1.5M I+D private/core
  - L3: 24MB/chip - shared
- 2 SC chips per MCM
  - L4: 2 x 96 M = 192 M L4 per book
  - SC Chip size 24.5 mm x 20.5 mm

–1800 Watts

## z196 Book Level Cache Hierarchy

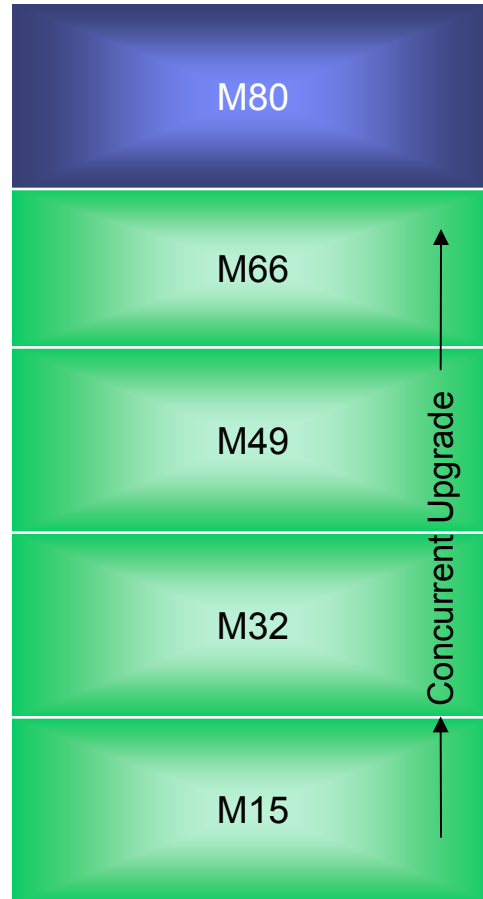
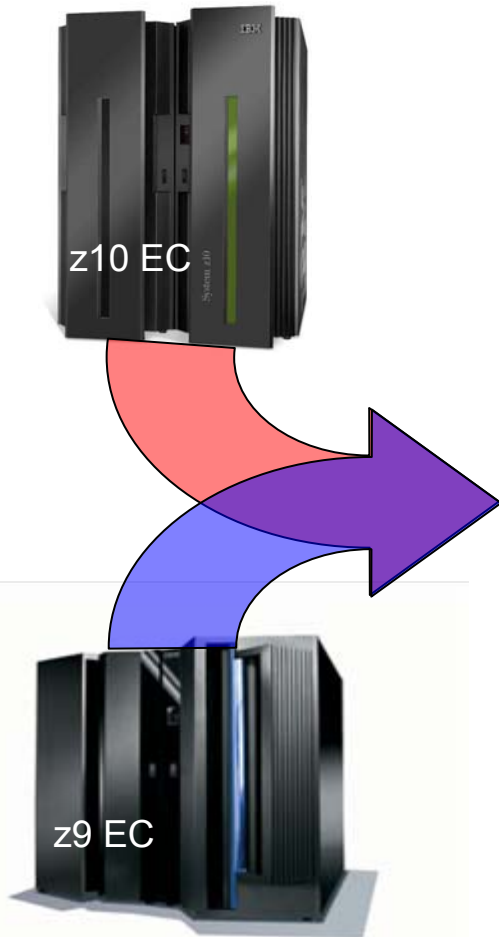


## z196 Air cooled – Under the covers (Model M66 or M80) Front view





## System Offering Overview



**z196**

### z196 machine type: 2817

#### Processors

- ▶ 20 or 24 available cores per book
- ▶ Sub-capacity available up to 15 CPs
  - ▶ 3 sub-capacity points
- ▶ 2 spares designated per system

#### Memory for customer purchase

- ▶ System minimum = 32 GB
  - ▶ 16 GB separate HSA
- ▶ Maximum: 3TB / 768 GB per book
- ▶ Increments: 32 to 256 GB

#### I/O Interconnects:

- ▶ At GA 6 GB/sec InfiniBand
- ▶ GA2: Add 8 GB/sec PCIe
- ▶ Up to 16 per book (8 fanouts)
- ▶ Up to 48 per CEC (24 fanouts)

#### ▶ Capacity compared to z10 EC

- ▶ z196 M80 compared to z10 EC E64 60% more capacity
- ▶ Equal “n-way” – 1.3 to 1.5 ITR ratio depending on workload
- ▶ Some workloads could gain up to 30% additional improvement if optimized to new z196 instructions and architecture

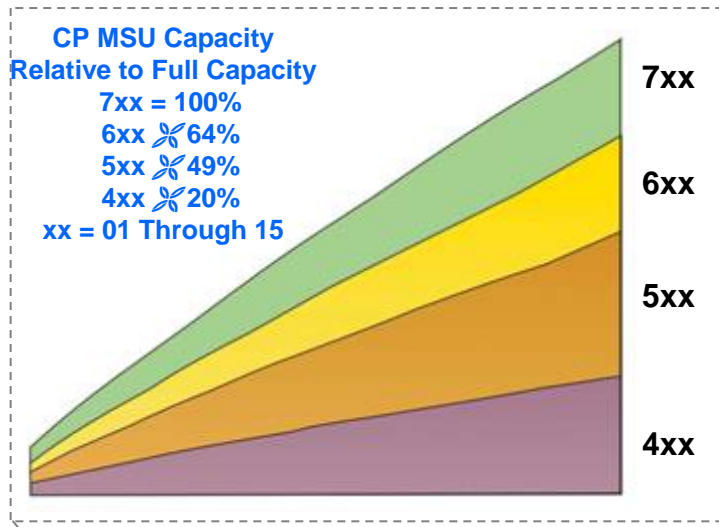
## z196 Processor Features

Model	Books/ PUs	CPs	IFLs uIFLs	zAAPs	zIIPs	ICFs	SAPs Std	Optional SAPs	Std. Spares
<b>M15</b>	<b>1/20</b>	<b>0-15</b>	<b>0-15 0-14</b>	<b>0-7</b>	<b>0-7</b>	<b>0-15</b>	<b>3</b>	<b>0-4</b>	<b>2</b>
<b>M32</b>	<b>2/40</b>	<b>0-32</b>	<b>0-32 0-31</b>	<b>0-16</b>	<b>0-16</b>	<b>0-16</b>	<b>6</b>	<b>0-10</b>	<b>2</b>
<b>M49</b>	<b>3/60</b>	<b>0-49</b>	<b>0-49 0-48</b>	<b>0-24</b>	<b>0-24</b>	<b>0-16</b>	<b>9</b>	<b>0-15</b>	<b>2</b>
<b>M66</b>	<b>4/80</b>	<b>0-66</b>	<b>0-66 0-65</b>	<b>0-33</b>	<b>0-33</b>	<b>0-16</b>	<b>12</b>	<b>0-20</b>	<b>2</b>
<b>M80</b>	<b>4/96</b>	<b>0-80</b>	<b>0-80 0-79</b>	<b>0-40</b>	<b>0-40</b>	<b>0-16</b>	<b>14</b>	<b>0-18</b>	<b>2</b>

- ▶ z196 Models M15 to M66 use books each with a 20 core MCM (two 4-core and four 3-core PU chips)
- ▶ Concurrent Book Add is available to upgrade from model to model (except to the M80)
- ▶ z196 Model M80 has four books each with a 24 core MCM (six 4-core PU chips)
- ▶ **Disruptive** upgrade to z196 Model M80 is done by book replacement

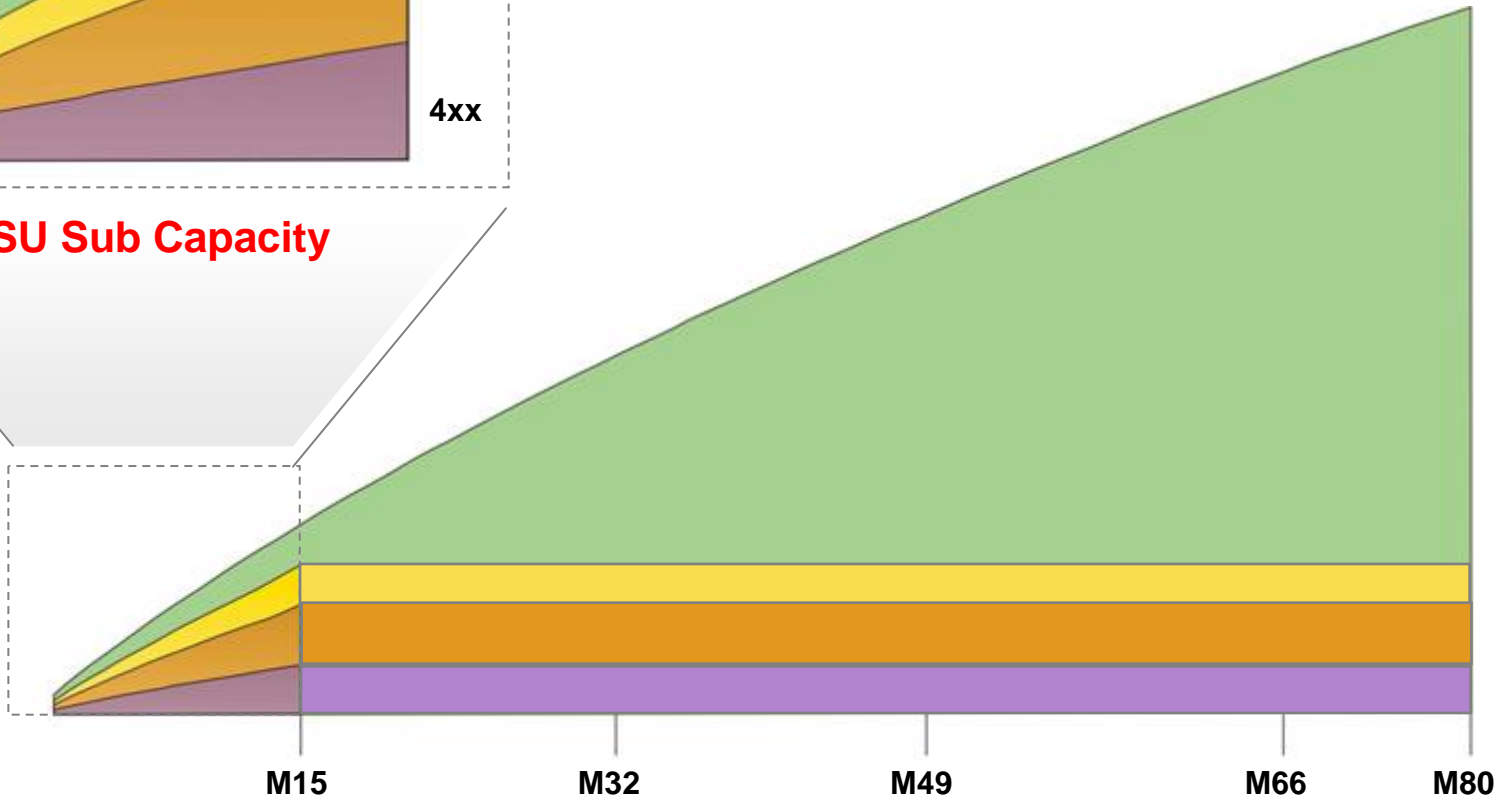
- Notes:
1. At least one CP, IFL, or ICF must be purchased in every machine
  2. One zAAP **and** one zIIP may be purchased for each CP purchased even if CP capacity is “banked”.
  3. “uFL” stands for Unassigned IFL

## z196 Full and Sub-Capacity CP Offerings



- **Subcapacity CPs, up to 15, may be ordered on ANY z196 model. If 16 or more CPs are ordered all must be full 7xx capacity**
- **All CPs on a z196 CEC must be the same capacity**
- **All specialty engines run at full capacity. The one for one entitlement to purchase one zAAP and one zIIP for each CP purchased is the same for CPs of any capacity.**
- **Only 15 CPs can have granular capacity but other PU cores may be characterized as full capacity specialty engines**

### MSU Sub Capacity

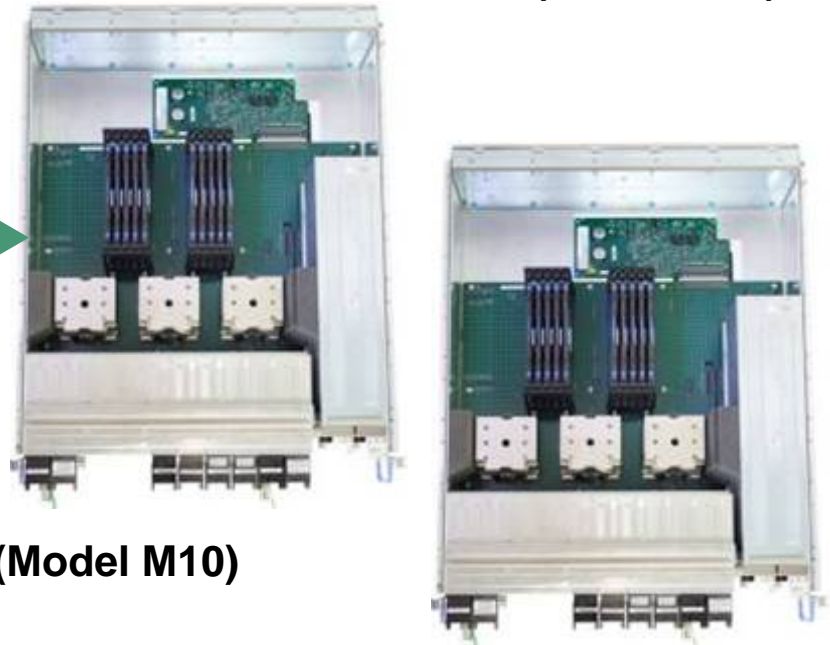


## Processor / Memory Subsystem Drawers (Model M05 and M10)

**One z10 BC Drawer**

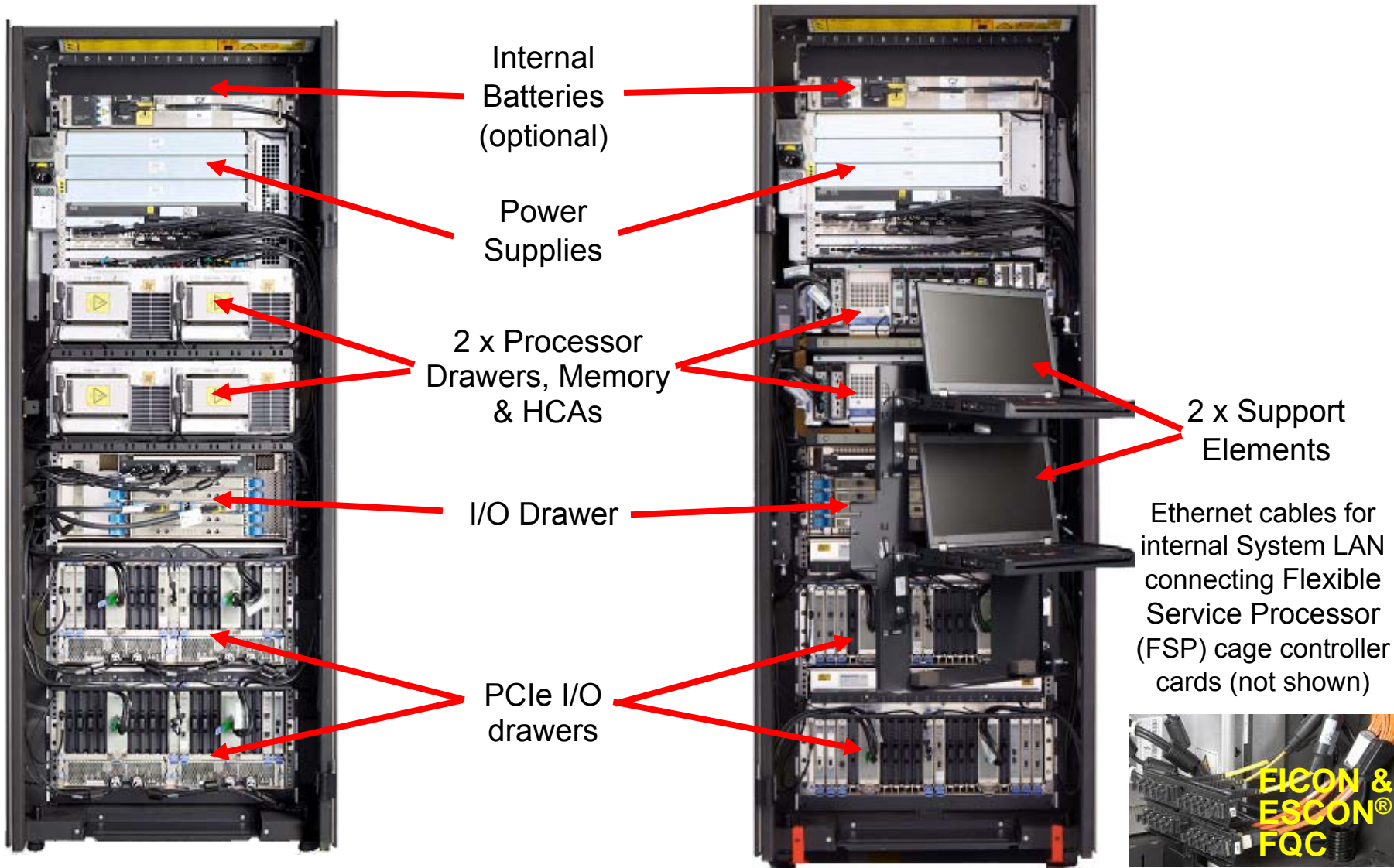


**Two z114 Drawers (Model M10)**



- **System resources split between 2 drawers (Model M10)**
- **Second CEC drawer (Model 10) for:**
  - Increased specialty engine capability
  - Increased memory capability
  - Increased I/O capability
    - More coupling links than z10 BC
    - More I/O features than z10 BC
- **Planning Note: Unlike the z196 Books, add/remove/repair of the CEC drawer is disruptive**

## z114 – Under the covers



## zEnterprise 114 Models M05 and M10

### ▪ M/T 2818 – Model M05

- Air cooled
- Single Frame
- Non-raised floor option available
- 30 LPARs

### ▪ Processor Units (PUs)

- New processor drawer design (1 CPC Drawer)
- 7 per system
  - 2 SAPs standard
  - Up to 5 CPs
  - Up to 5 specialty engines
  - Up to 2 zIIPs/zAAPs
  - 0 spares when fully configured

### • Memory 8 GB to 120 GB

### ▪ M/T 2818 – Model M10

- Air cooled
- Single Frame
- Non-raised floor option available
- 30 LPARs

### ▪ Processor Units (PUs)

- New processor drawer design (2 CPC Drawers)
- 14 per system
  - 2 SAPs standard
  - Up to 5 CPs
  - Up to 10 specialty engines
  - Up to 5 zIIPs/zAAPs
  - 2 dedicated spares

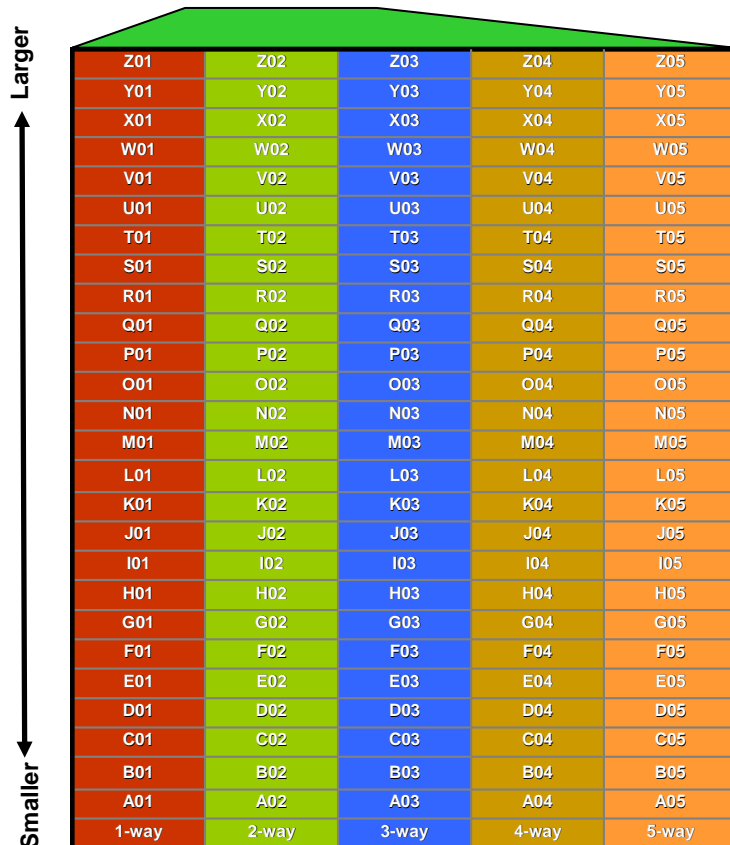
### ▪ Memory 16 GB to 248 GB

### ▪ Why a Model M10? (Two CPC drawers)

- > 5 Customer PUs
- > 120 GB memory
- > 4 Fanouts for additional I/O connectivity – especially PSIFB links
  - Depends - numbers vary for drawers, I/O features and PSIFB links

Designed and right-sized for existing and future applications requirements

	CP	IFL	zIIP	zAAP	ICF	Add'l SAP	Std SAP	Spare
M05	0-5	0-5	0-2	0-2	0-5	0-2	2	0
M10	0-5	0-10	0-5	0-5	0-10	0-2	2	2



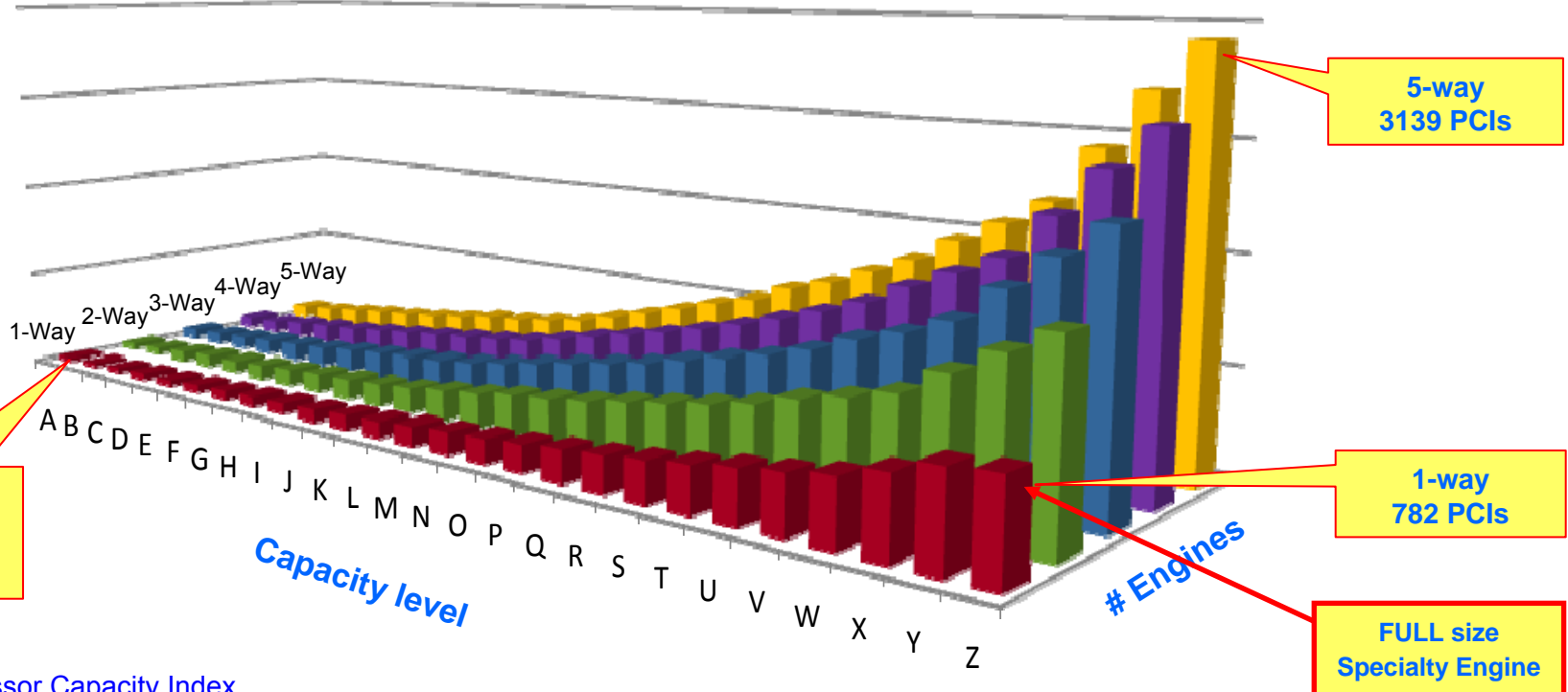
Z01	Z02	Z03	Z04	Z05
Y01	Y02	Y03	Y04	Y05
X01	X02	X03	X04	X05
W01	W02	W03	W04	W05
V01	V02	V03	V04	V05
U01	U02	U03	U04	U05
T01	T02	T03	T04	T05
S01	S02	S03	S04	S05
R01	R02	R03	R04	R05
Q01	Q02	Q03	Q04	Q05
P01	P02	P03	P04	P05
O01	O02	O03	O04	O05
N01	N02	N03	N04	N05
M01	M02	M03	M04	M05
L01	L02	L03	L04	L05
K01	K02	K03	K04	K05
J01	J02	J03	J04	J05
I01	I02	I03	I04	I05
H01	H02	H03	H04	H05
G01	G02	G03	G04	G05
F01	F02	F03	F04	F05
E01	E02	E03	E04	E05
D01	D02	D03	D04	D05
C01	C02	C03	C04	C05
B01	B02	B03	B04	B05
A01	A02	A03	A04	A05
1-way	2-way	3-way	4-way	5-way

- Complete capacity matrix available on both models.
- Granularity levels similar to z10 BC to facilitate upgrades and incremental growth
- Model M10 provides specialty engine scale out capabilities
- Any to any capacity upgrade/downgrade capability within the Model
- CBU capability from smallest to largest capacities within the Model
- On/Off CoD within the Model
- Linux only and ICF only servers

## z114 Sub-capacity Processor Granularity

- **The z114 has 26 CP capacity levels (26 x 5 = 130)**
  - Up to 5 CPs at any capacity level
    - All CPs must be the same capacity level
- **The one for one entitlement to purchase one zAAP and/or one zIIP for each CP purchased is the same for CPs of any speed.**
  - All specialty engines run at full capacity
  - Processor Unit Value for IFL = 100

Number of z114 CPs	Base Ratio	Ratio z114 to z10 BC
1 CP	z10 BC Z01	1.18
2 CPs	z10 BC Z02	1.16
3 CPs	z10 BC Z03	1.14
4 CPs	z10 BC Z04	1.13
5 CPs	z10 BC Z05	1.12

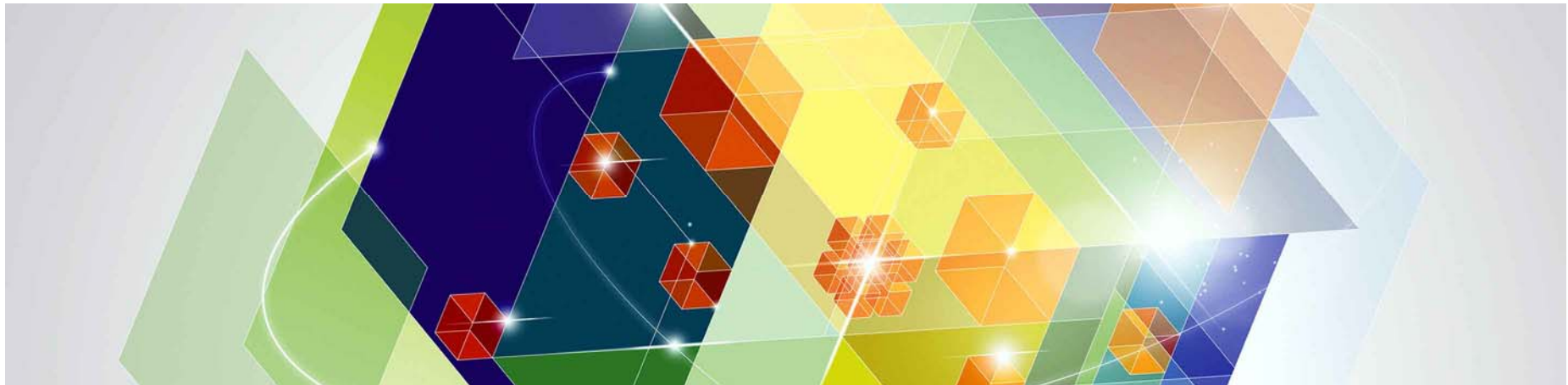


PCI – Processor Capacity Index



## zEnterprise Memory

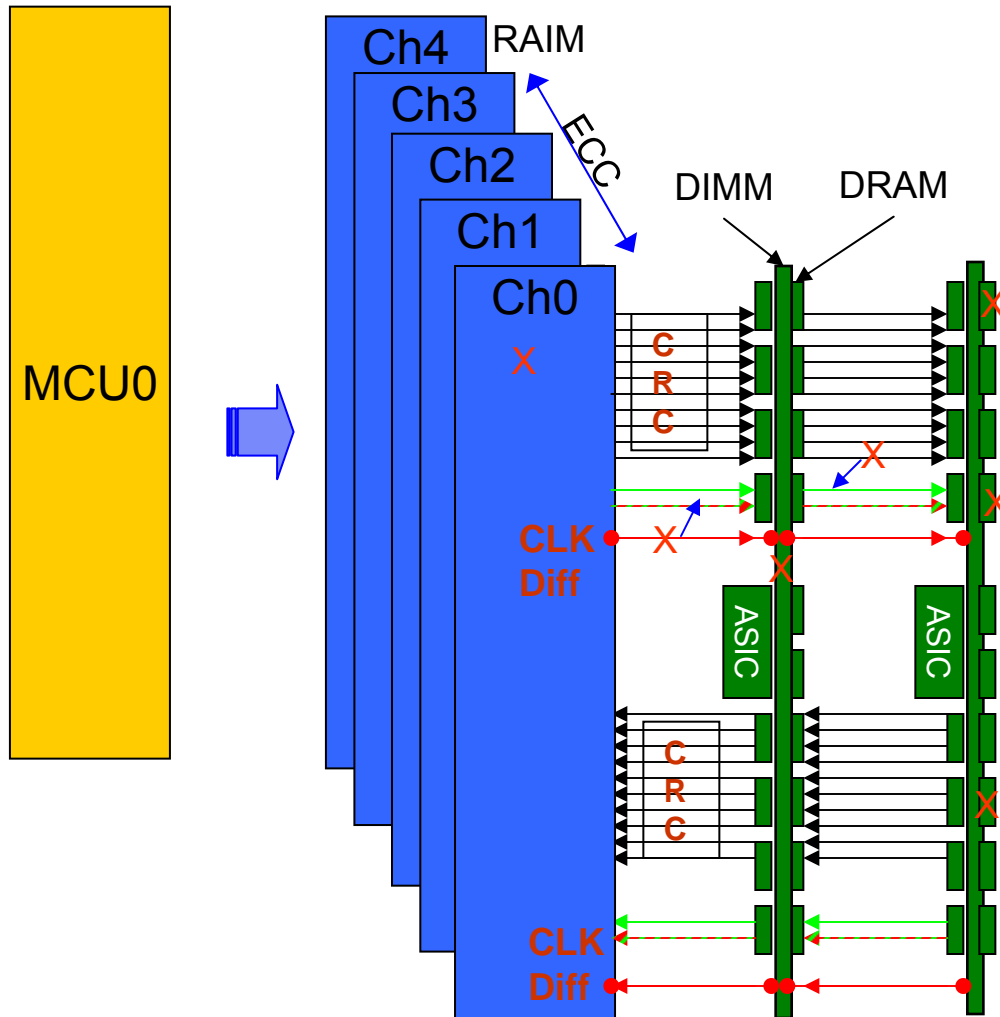
System z – Freedom Through Design



## z196 Redundant Array of Independent Memory (RAIM)

- **System z10 EC memory design:**
  - Four Memory Controllers (MCUs) organized in two pairs, each MCU with *four* channels
  - DIMM technology is Nova x4, 16 to 48 DIMMs per book, plugged in groups of 8
  - 8 DIMMs (4 or 8 GB) per feature – 32 or 64 GB physical memory per feature  
Equals 32 or 64 GB for HSA and customer purchase per feature
  - 64 to 384 GB physical memory per book = *64 to 384 GB for use (HSA and customer)*
  
- **z196 memory design:**
  - Three MCUs, each with *five* channels. The fifth channel in each z196 MCU is required to implement memory as a *Redundant Array of Independent Memory (RAIM)*. *This technology adds significant error detection and correction capabilities. Bit, lane, DRAM, DIMM, socket, and complete memory channel failures can be detected and corrected, including many types of multiple failures.*
  - DIMM technology is SuperNova x81, 10 to 30 DIMMs per book, plugged in groups of 5  
5 DIMMs (4, 16 or 32 GB) per feature – 20, 80 or 160 GB physical RAIM per feature  
Equals 16, 64 or 128 GB for use per feature. *RAIM takes 20%. (There is no non-RAIM option.)*
  - 40 to 960 GB RAIM memory per book = *32 to 768 GB of memory for use*  
(Minimum RAIM for the M15 is 60 GB = 48 GB = 16 GB HSA plus 32 GB customer memory)
  
- **For both z196 and z10 EC**
  - *The Hardware System Area (HSA) is 16 GB fixed, outside customer memory*
  - *In some cases, offering granularity can prevent purchase of all available memory in a book*

## z196 RAIM Memory Controller Overview



2- Deep Cascade  
Using Quad High DIMMs

SHARE 118 in Atlanta, March 13, 2012

### Layers of Memory Recovery

#### ECC

- Powerful 90B/64B Reed Solomon code

#### DRAM Failure

- Marking technology; no half sparing needed
- 2 DRAM can be marked
- Call for replacement on third DRAM

#### Lane Failure

- CRC with Retry
- Data – lane sparing
- CLK – RAIM with lane sparing

#### DIMM Failure (discrete components, VTT Reg.)

- CRC with Retry
- Data – lane sparing
- CLK – RAIM with lane sparing

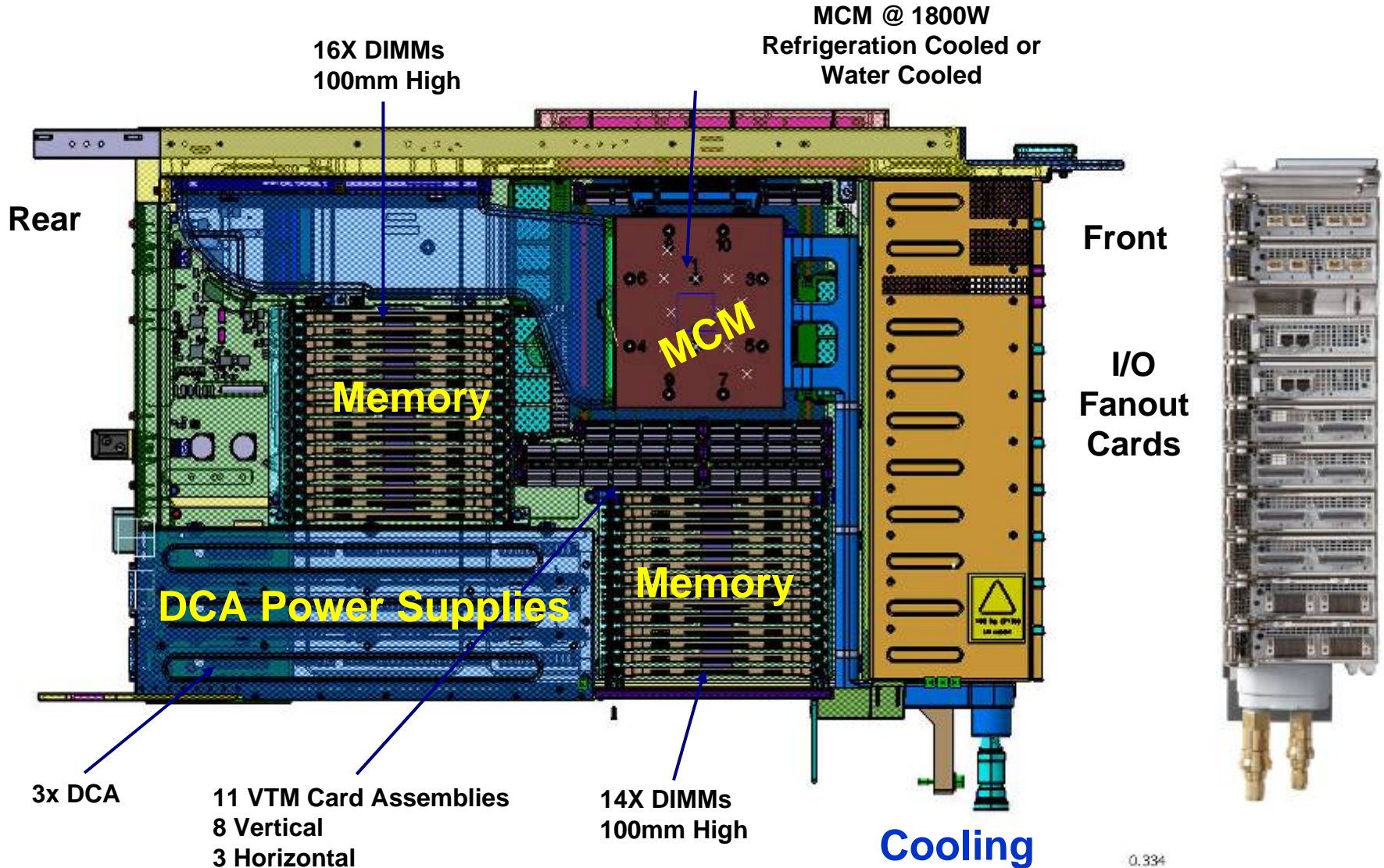
#### DIMM Controller ASIC Failure

- RAIM Recovery

#### Channel Failure

- RAIM Recovery

## z196 Book Layout



## z196 Purchase Memory Offerings

Model	Standard Memory GB	Flexible Memory GB
M15	32 - 704	NA
M32	32 - 1520	32 - 704
M49	32 - 2288	32 - 1520
M66	32 - 3056	32 - 2288
M80	32 - 3056	32 - 2288

- **Purchase Memory** - Memory available for assignment to LPARs
- **Hardware System Area** – Standard 16 GB outside customer memory for system use
- **Standard Memory** - Provides minimum physical memory required to hold base purchase memory plus 16 GB HSA
- **Flexible Memory** - Provides additional physical memory needed to support activation base customer memory and HSA on a multiple book z196 with one book out of service.
- **Plan Ahead Memory** – Provides additional physical memory needed for a concurrent upgrade (LIC CC change only) to a preplanned target customer memory

## z196 Flexible Memory

- **Provides additional physical memory needed to support activation all purchased memory and HSA on a multiple book z196 with one book out of service for**
  - Scheduled concurrent upgrades that take a book temporarily out of service. This includes memory upgrades that add or change memory DIMMSs
  - Scheduled concurrent repairs that take a book temporarily out of service to replace a component.
  - Concurrent repair of a book “fenced” (placed out of service) during Activation (POR)
  - *Note: All of the above can be done without Flexible Memory; but, all purchased memory will not be available for use in most cases. Some work may have to be shut down or not restarted.*
  
- **Offered on M32, M49, M66 and M80 in:**
  - 32 GB increments from 32 GB to 256 GB
  - 64 GB increments from 320 GB to 512 GB
  - 96 GB increments from 608 GB to 896 GB (*M32 limit 704 GB*)
  - 112 GB increment to 1008 GB
  - 128 GB increments from 1136 GB to 1520 GB (*M49 limit 1520 GB*)
  - 256 GB increments from 1776 GB to 2288 GB
  
- **Selected by checking the “Flexible” box when configuring memory**
  
- **Additional physical memory, if required, is added to the configuration and priced as “Plan Ahead Memory”**

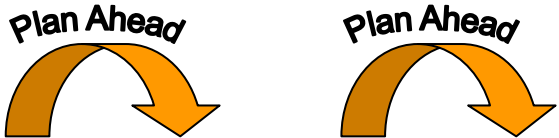
## z196 Standard and Flexible Purchase Memory Offerings

Increment	GB, Notes	Growth %	Increment	GB, Notes	Growth %	Increment	GB, Notes	Growth %
32 GB	32	100%	96 GB	608	16%	256 GB	1776	17%
	64	50%		704 <sup>1</sup>	13%		2032	13%
	96	33%		800	12%		2288 <sup>3</sup>	11%
	128	25%		896	12%		2544	10%
	160	20%					2800	9%
	192	17%	112 GB	1008	13%		3056 <sup>4</sup>	NA
	224	14%						
	256	25%						
						<p><b>Notes – Memory Maximums:</b></p> <p>1. M15 Standard, M32 Flexible = 704</p> <p>2. M32 Standard, M49 Flexible, (z10 EC Standard)= 1520</p> <p>3. M49 Standard, M66 and M80 Flexible = 2288</p> <p>4. M66 and M80 Standard = 3056</p>		
64 GB	320	20%	128 GB	1136	11%			
	384	17%		1264	10%			
	448	14%		1392	9%			
	512	19%		1520 <sup>2</sup>	17%			

## z114 Model M05 Memory Features

### Plan Ahead Memory

- Pre-plugged memory based on target capacity specified by the customer.
- Enabled by LICCC, concurrently.
- **FC1993** tracks the quantity of 8GB physical increments.
  - Charged (half price) when physical memory is installed
- **FC1903** generally indicates 8GB (or 32 GB in larger configurations) LICC'd increments of Memory Capacity.
  - Charged by increments when Plan Ahead memory is enabled
  - Subsequent memory upgrade orders will use up the Plan Ahead memory first.



10 x 4 GB DIMMs	10 x 8 GB DIMMs	10 x 16 GB DIMMs
Feature Size	Feature Size	Feature Size
8	32	64
16	40	72
24	48	80
	56	88
		96
		104
		112
		120

Physical memory upgrades are *DISRUPTIVE*



## z114 Model M10 Memory Features

Drawer 1/ Drawer 2

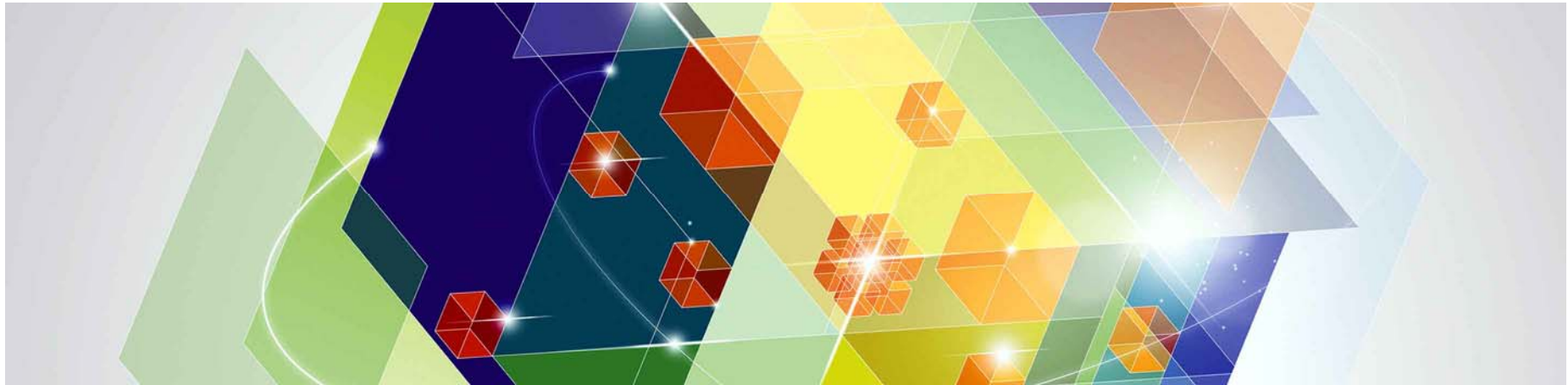


4 GB/4GB	4GB/8GB 8GB/4GB	8GB/8GB	4GB/16GB 16GB/4GB	8GB/16GB 16GB/8GB	16GB/16GB
Feature Size	Feature Size	Feature Size	Feature Size	Feature Size	Feature Size
16	64	96	152	184	216
24	72	104			248
32	80	112			
40	88	120			
48					
56					

Physical memory upgrades are a *DISRUPTIVE*

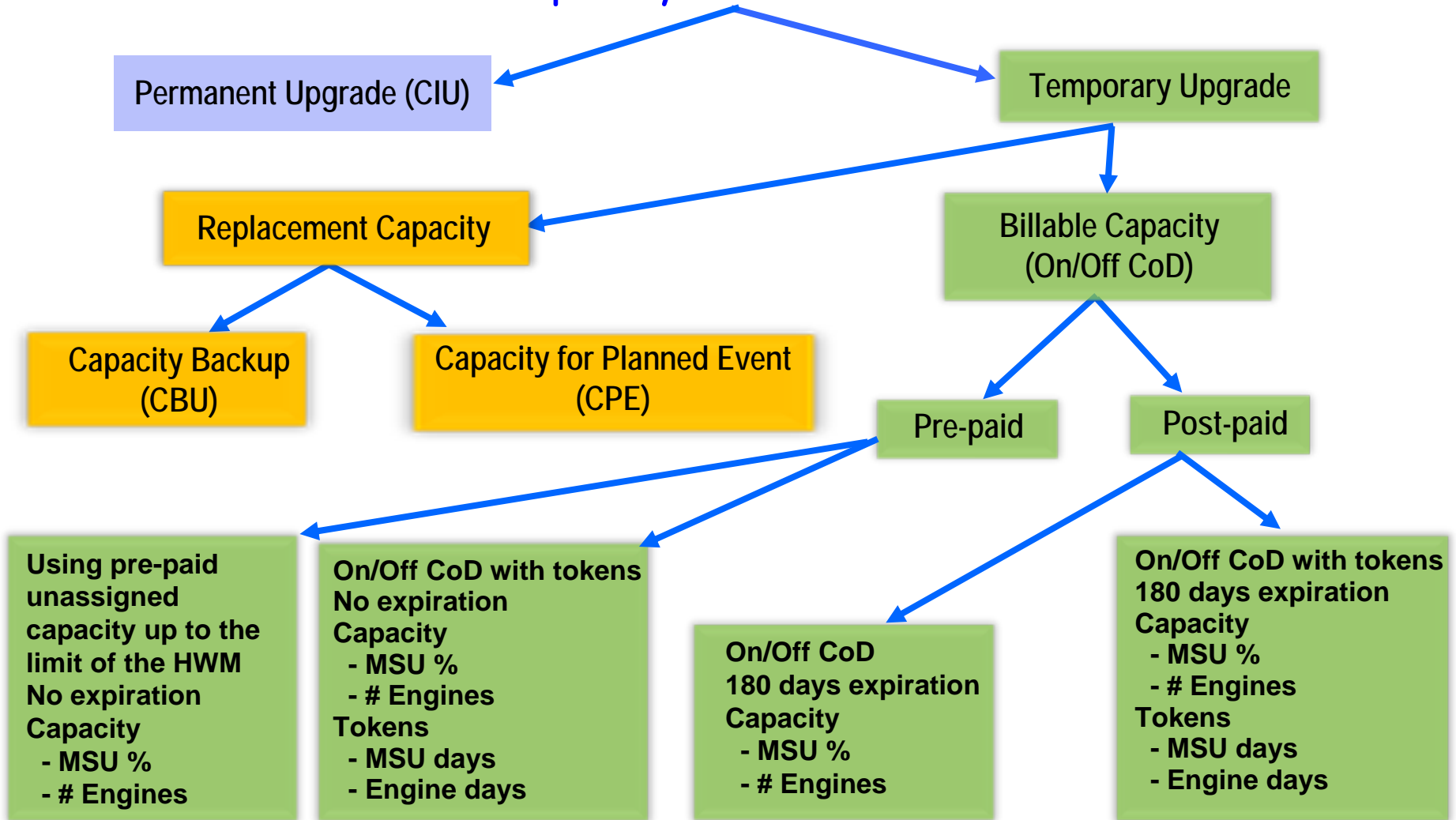
# zEnterprise 196 On Demand Capabilities

System z – Freedom Through Design



## zEnterprise Basics of Capacity on Demand

### Capacity on Demand

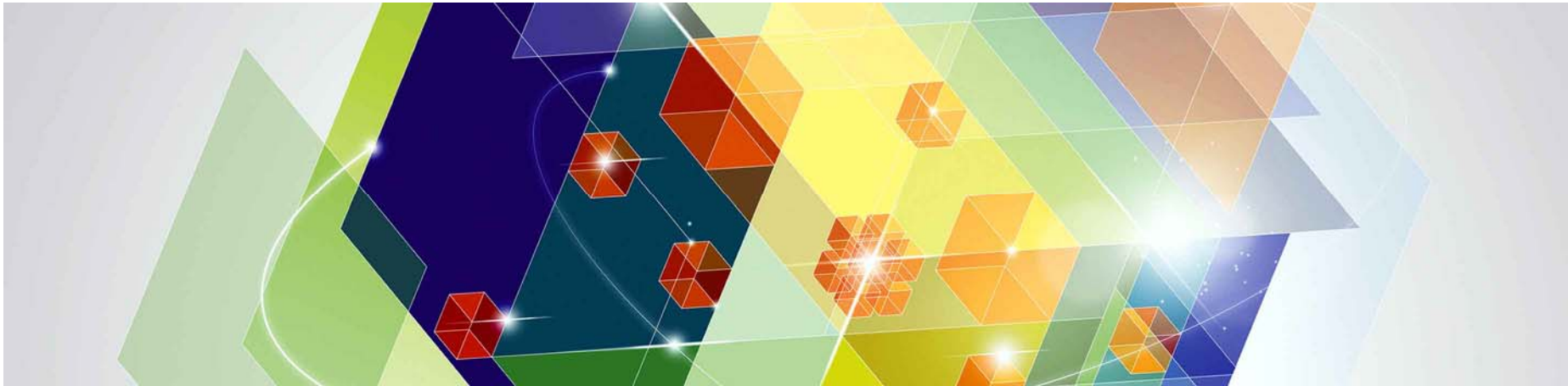


## zEnterprise Capacity on Demand Exclusives

- **On/Off Capacity on Demand (On/Off CoD) Improvements**
  - **Auto Replenishment of On/Off CoD records**
    - Automatic extension of the expiration date of installed On/Off CoD records
  - **On/Off CoD Administrative Test**
    - On/Off CoD “zero capacity” records for testing and training
  
- **CIU Improvement**
  - **Purchase of permanent unassigned engines**
    - On permanent engine purchased, Resource Link will provide the customer with the options to adjust the active capacity mark
  
- **Pre Installed Capacity Backup and Capacity for Planned Event Records**
  - Systems manufactured with records installed instead of staged to the Support Element
  - Limitation: Only up to 4 records can be installed  
(Note: This limitation will effect very few orders.)
  
- **Miscellaneous Panel Enhancements**
  - Add Capacity Level Increase (CLI) to panels aka. “Speed Steps”
  - Warning for “Last Real Activation” for CBU
  - Peak Usage Marks for processor & MSU tokens (“consumption rate

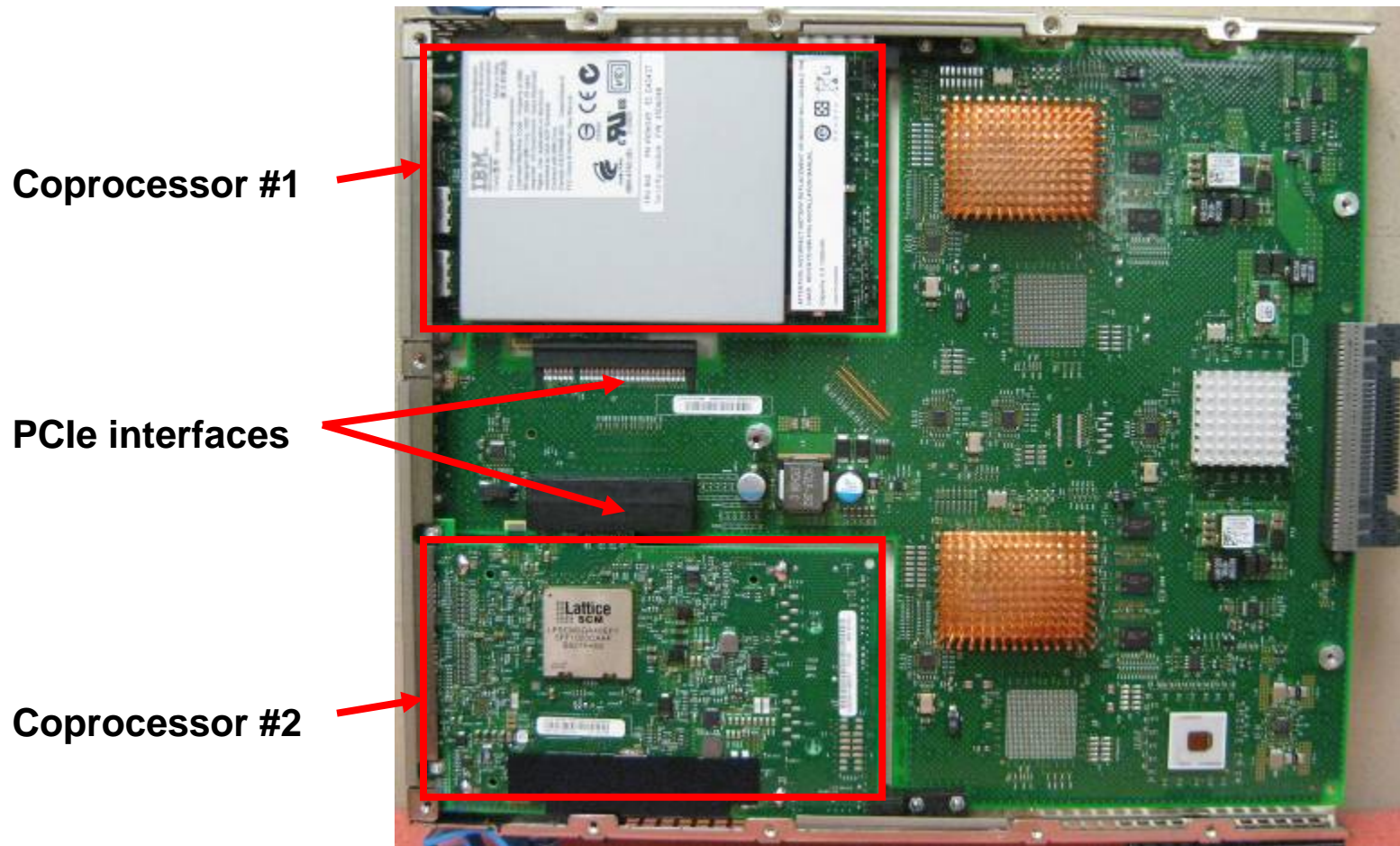
# zEnterprise Cryptographic Capabilities

## System z – Freedom Through Design



## Crypto Express3 2-P (View inside the feature card)

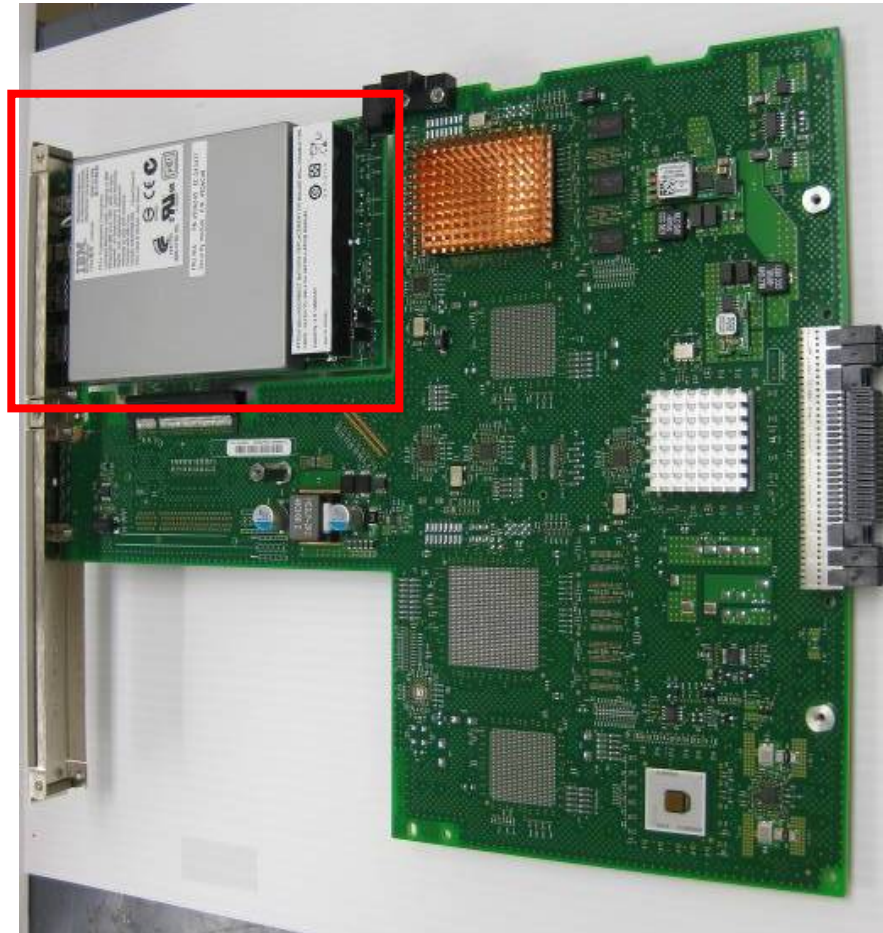
- Earlier cryptographic features not supported
- Supported: 0, 2, 3 – 8 features = 0, 4, 6 – 16 cryptographic engines.  
Each can be individually configured as Coprocessor or Accelerator.



## Crypto Express3 1-P (View inside the feature card)

- **Crypto Express3 1-P card with one coprocessor**
  - Available on z114 only in addition to the Crypto Express3 2-P
  - Supported: 0, 2, 3 – 8 features = 0, 2, 3 – 16 cryptographic engines.

Coprocessor #1



## Exclusive zEnterprise cryptographic capabilities (July 22, 2010)

- **Elliptic Curve Cryptography Digital Signature Algorithm**, an emerging public key algorithm expected eventually to replace RSA cryptography in many applications. ECC is capable of providing digital signature functions and key agreement functions. The new CCA functions provide ECC key generation and key management and provide digital signature generation and verification functions compliance with the ECDSA method described in **ANSI X9.62 "Public Key Cryptography for the Financial Services Industry: The Elliptic Curve Digital Signature Algorithm (ECDSA) "**. ECC uses keys that are shorter than RSA keys for equivalent strength-per-key-bit; RSA is impractical at key lengths with strength-per-key-bit equivalent to AES-192 and AES-256. So the strength-per-key-bit is substantially greater in an algorithm that uses elliptic curves.
- **ANSI X9.8 PIN security** which facilitates compliance with the processing requirements defined in the new version of the **ANSI X9.8 and ISO 9564 PIN Security Standards** and provides added security for transactions that require Personal Identification Numbers (PIN).
- **Enhanced Common Cryptographic Architecture (CCA)**, a Common Cryptographic Architecture (CCA) key token wrapping method using Cipher Block Chaining (CBC) mode in combination with other techniques to satisfy the key bundle compliance requirements in standards including **ANSI X9.24-1** and the recently published **Payment Card Industry Hardware Security Module (PCI HSM) standard**.
- **Secure Keyed-Hash Message Authentication Code (HMAC)**, a method for computing a message authentication code using a secret key and a secure hash function. It is defined in the standard **FIPS 198, "The Keyed-Hash Message Authentication Code "**. The new CCA functions support HMAC using SHA-1, SHA-224, SHA-256, SHA-384, and SHA-512 hash algorithms. The HMAC keys are variable-length and are securely encrypted so that their values are protected.
- **Modulus Exponent (ME) and Chinese Remainder Theorem (CRT)**, RSA encryption and decryption with key lengths greater than 2048-bits and up to 4096-bits.



## Summary of Cryptographic Enhancements (July 12, 2011)

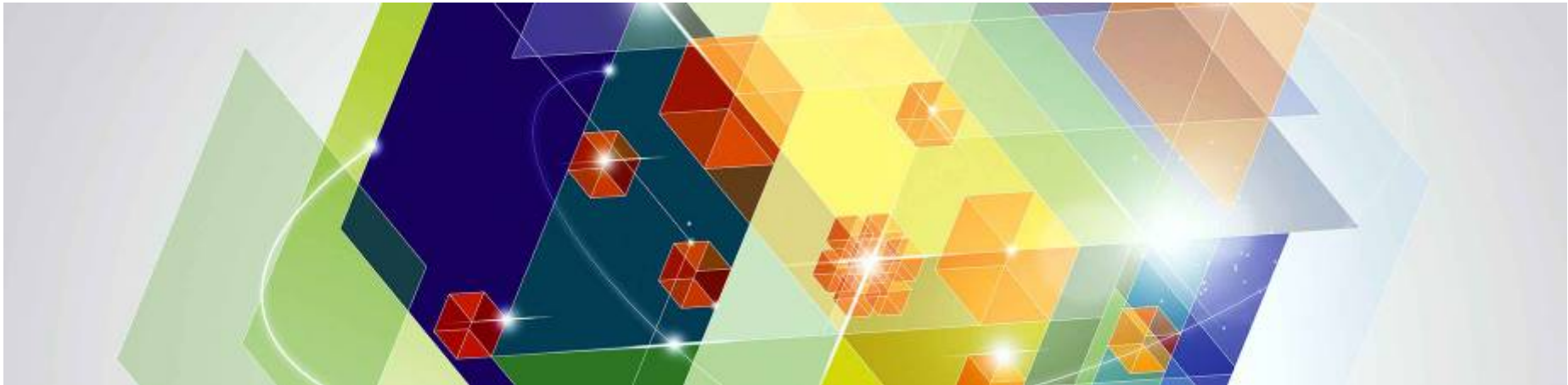


- **Crypto Express3-1P (z114 only):** A cost reduced one coprocessor version of Crypto-Express3
- **Expanded key support for the AES algorithm:** Adds support for **AES Key Encrypting Keys (AES KEKs) and AES typed keys**. These AES wrapping keys have adequate strength to protect other AES keys for transport or storage. The new AES key types use the variable-length key token. The supported key types are EXPORTER, IMPORTER, and for use in the encryption and decryption services, CIPHER.
- **Enhanced ANSI TR-31 interoperable secure key exchange.** **ANSI TR-31** key wrapping defines a method of cryptographically protecting Triple Data Encryption Standard (TDES) cryptographic keys and their associated usage attributes.
- **Elliptic Curve Cryptography (EC-DH key agreement protocol):** **EC-DH key agreement protocol** allows two parties, each having an elliptic curve public-private key pair, to establish a shared secret over an insecure channel. This shared secret may be used directly as a key, or to derive another key which can then be used to encrypt subsequent communications using a symmetric key cipher such as AES.
- **PIN block decimalization table protection:** To help avoid a decimalization table attack to learn a personal identification number (PIN), a solution is now available in the CCA API to thwart this attack by protecting the decimalization table from manipulation.
- **PKA RSA OAEP with SHA-256:** **Optimal Asymmetric Encryption Padding (RSA OAEP)** is a public-key encryption scheme or method of encoding messages and data in combination with the RSA algorithm and a hash algorithm.

## z196 and z114 I/O Structure

More detail in Session 10617  
Tuesday, 4:30 PM, International Ballroom C

System z – Freedom Through Design



## The zEnterprise 114 and zEnterprise 196 GA2 I/O Infrastructure



### New PCIe-based I/O infrastructure

- **New PCIe-based 8 GBps interconnects**
- **New PCIe I/O drawer**
  - Improved port purchase granularity (fewer ports per I/O card)
  - Increased port density compared to the previous I/O drawer or z196 I/O cage
  - Designed for improved power and bandwidth compared to previous I/O cage or z196 I/O drawer

### Storage

- **New PCIe-based FICON Express8S** features

### Networking

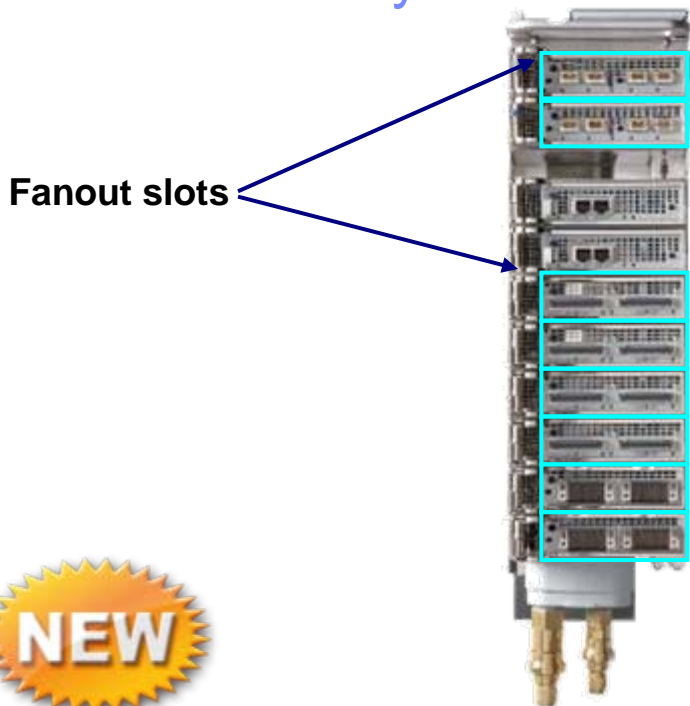
- **New PCIe-based OSA-Express4S** features

### Coupling

- **New** 12x InfiniBand and 1x InfiniBand features (**HCA3-O fanouts**)
  - *12x InfiniBand - decreased service times when using 12x IFB3 protocol*
  - *1x InfiniBand – increased port count and more subchannels per CHPID*

**Note: The z114 and z196 at GA2 will ship with a new LIC Driver, Driver 93g**

## z196 Connectivity for I/O and Coupling

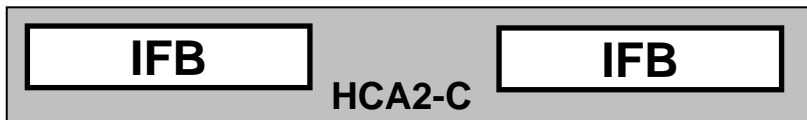
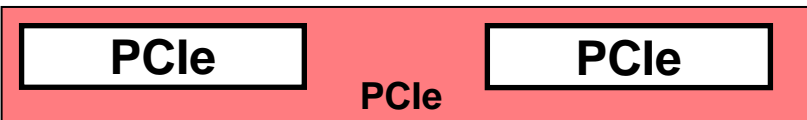


- **Up to 8 fanout cards per z196 book**
  - M15 (1 book) – up to 8
  - M32 (2 books) – up to 16
  - M49 (3 books) – up to 20
  - M66 and M80 (four books) – up to 24

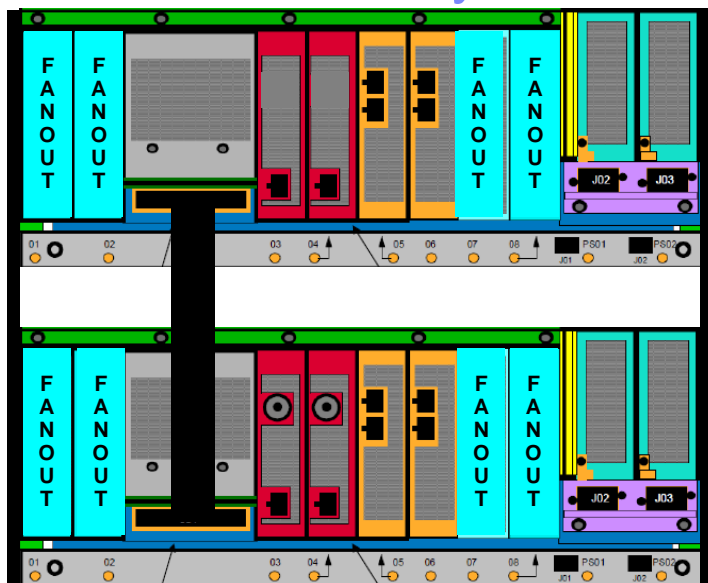
- **I/O fanouts compete for fanout slots with the the InfiniBand HCA fanouts that support coupling:**
  - HCA2-O 12x two InfiniBand DDR links
  - HCA2-O LR two 1x InfiniBand DDR links
  - **HCA3-O two 12x InfiniBand DDR links**
  - **HCA3-O LR four 1x InfiniBand DDR links**

- **PCIe fanout – PCIe I/O Interconnect links**  
 Supports two copper cable PCIe 8 GBps interconnects to two 8-card PCIe I/O domain multiplexers.  
**Always plugged in pairs for redundancy.**

- **HCA2-C fanout – InfiniBand I/O Interconnect**  
 Supports two copper cable 12x InfiniBand DDR 6 GBps interconnects to two 4-card I/O domain multiplexers.  
**Always plugged in pairs for redundancy.**



## z114 Connectivity for I/O and Coupling

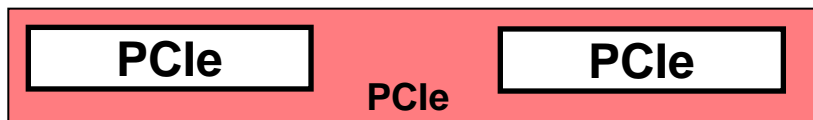


Drawer 2  
M10 only

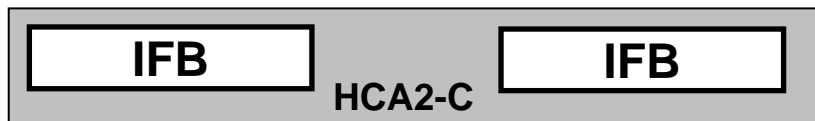
- Up to 4 fanouts per z114 CEC drawer
  - M05 (one CEC drawer) – up to 4 fanouts
  - M10 (two CEC drawers) – up to 8 fanouts

Drawer 1  
M05 and M10

- I/O fanouts compete for fanout slots with the InfiniBand HCA fanouts that support coupling:
  - HCA2-O 12x two InfiniBand DDR links
  - HCA2-O LR two 1x InfiniBand DDR links
  - HCA3-O two 12x InfiniBand DDR links**
  - HCA3-O LR four 1x InfiniBand DDR links**



- PCIe fanout – PCIe I/O Interconnect links**  
Supports two PCIe 8 GBps interconnects on copper cables to two 8-card PCIe I/O domain switches.  
**Always plugged in pairs for redundancy.**



- HCA2-C fanout – InfiniBand I/O Interconnect**  
Supports two 12x InfiniBand DDR 6 GBps interconnects on copper cables to two 4-card I/O domain multiplexers.  
**Always plugged in pairs for redundancy.**

## z196 GA2 I/O Features supported

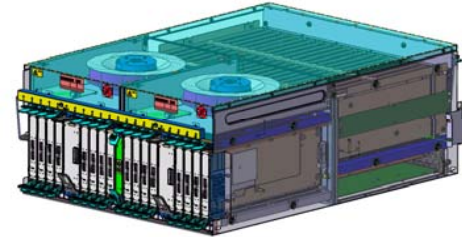
### Supported features

#### ■ Features – PCIe I/O drawer

- **FICON Express8S**
  - SX and LX
- **OSA-Express4S**
  - 10 GbE LR and SR
  - GbE SX and LX



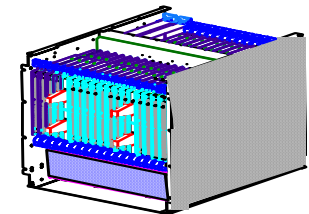
PCIe I/O drawer



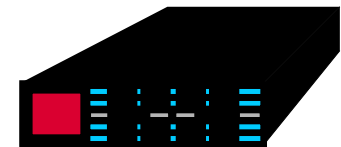
32 I/O slots

#### ■ Features – I/O cage and I/O drawer

- **Crypto Express3**
- **ESCON (240 or fewer)**
- FICON Express8 (*Carry forward or RPQ 8P2534 to fill empty slots*)
- FICON Express4 (*Carry forward only*)
- **ISC-3**
- **OSA-Express3 1000BASE-T**
- OSA-Express3 (*Carry forward or RPQ 8P2534 to fill empty slots*)
  - 10 GbE, GbE
- OSA-Express2 (*Carry forward only*)
  - GbE, 1000BASE-T
- **PSC (Carry forward or new build, no MES add)**



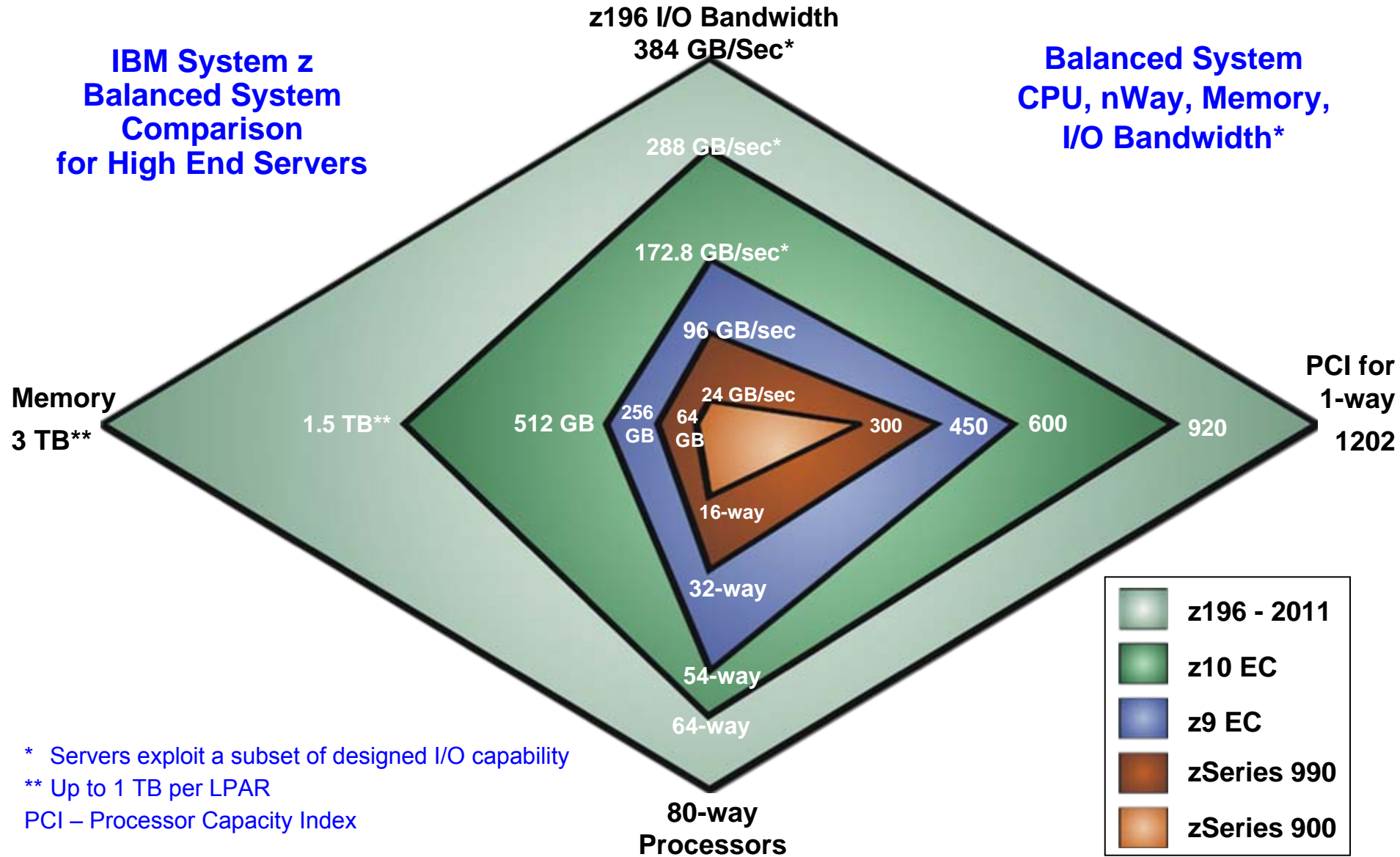
28 slot I/O cage  
**(z196 ONLY)**



8 slot I/O drawer

## IBM System z Balanced System Comparison for High End Servers

## Balanced System CPU, nWay, Memory, I/O Bandwidth\*



\* Servers exploit a subset of designed I/O capability

\*\* Up to 1 TB per LPAR

PCI – Processor Capacity Index

## z196 GA2 I/O Connectivity

Features	Offered As	Maximum # of features	Maximum channels	Increments per feature	Purchase increments
<b>ESCON</b>	<b>NB</b>	16	240 channels	1 - 15 active	4 channels
<b>FICON</b>					
<i>FICON Express8S</i>	<i>NB</i>	<i>160</i>	<i>320 channels</i>	<i>2 channels</i>	<i>2 channels</i>
<i>FICON Express8</i>	<i>CF*</i>	<i>72</i>	<i>288 channels</i>	<i>4 channels</i>	<i>4 channels</i>
<i>FICON Express4</i>	<i>CF</i>	<i>72</i>	<i>288 channels</i>	<i>4 channels</i>	<i>4 channels</i>
<b>ISC-3</b>	<b>NB</b>	12	48 links	4 links	1 link
<b>OSA-Express</b>					
<b>OSA-Express4S</b>	<b>NB</b>	48	96 ports	1 (10 GbE) / 2 ports	1 feature
<b>OSA-Express3 1000BASE-T</b>	<b>NB</b>	24	96 ports	4 ports	1 feature
<i>OSA-Express3 10 GbE, GbE</i>	<i>CF*</i>	<i>24</i>	<i>96 ports</i>	<i>2 (10 GbE) / 4 ports</i>	<i>1 feature</i>
<i>OSA-Express2**</i>	<i>CF*</i>	<i>24</i>	<i>48 ports</i>	<i>2 ports</i>	<i>1 feature</i>
<b>Crypto Express3***</b>	<b>NB</b>	8	16 PCIe adapters	2 PCIe adapters	1 feature ***

\* Can be carried forward or ordered on MES with RPQ 8P2534 if adding PCIe features is not possible

\*\* OSA-Express2 10 GbE LR is not supported as a carry forward

\*\*\* Two features initially, one thereafter

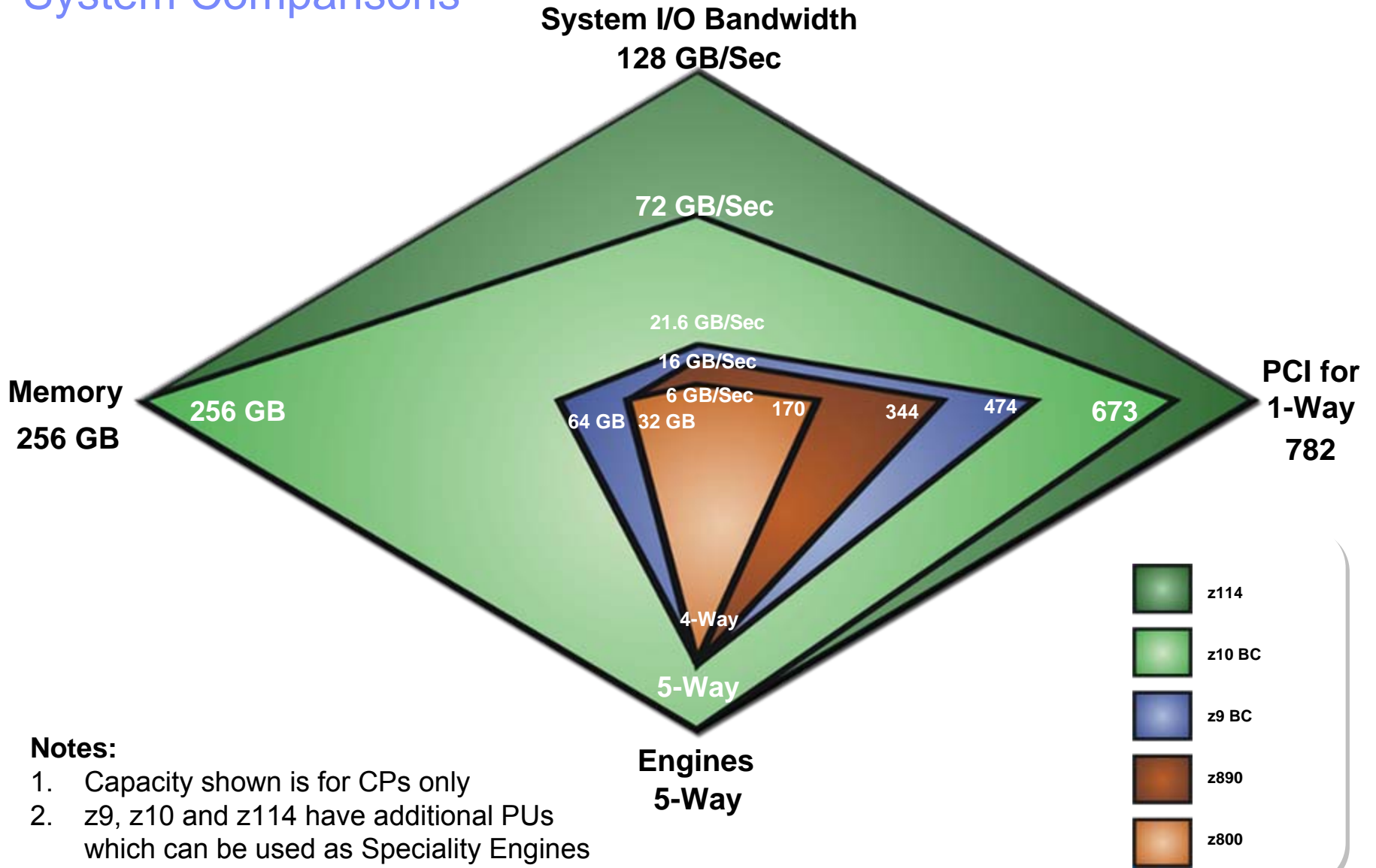
**NB = New Build**

*CF = Carry Forward*

\* All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of General Direction is at the relying party's sole risk and will not create liability or obligation for IBM.



## System Comparisons



## z114 I/O Connectivity

Features	Offered As	Maximum # of features	Maximum channels	Increments per feature	Purchase increments
<b>ESCON</b>	<b>NB</b>	16	240 channels	1 - 15 active	4 channels
<b>FICON</b>					
<b>FICON Express8S</b>	<b>NB</b>	64	128 channels	2 channels	2 channels
<i>FICON Express8</i>	<i>CF*</i>	<i>16</i>	<i>64 channels</i>	<i>4 channels</i>	<i>4 channels</i>
<i>FICON Express4</i>	<i>CF</i>	<i>16</i>	<i>64 channels</i>	<i>4 channels</i>	<i>4 channels</i>
<i>FICON Express4-2C</i>	<i>CF*</i>	<i>16</i>	<i>32 channels</i>	<i>2 channels</i>	<i>2 channels</i>
<b>ISC-3</b>	<b>NB</b>	12	48 links	4 links	1 link
<b>OSA-Express</b>					
<b>OSA-Express4S</b>	<b>NB</b>	48	96 ports	1 (10 GbE) / 2 ports	1 feature
<b>OSA-Express3 1000BASE-T</b>	<b>NB</b>	16	64 ports	2 (-2P) / 4 ports	1 feature
<i>OSA-Express3 10 GbE, GbE</i>	<i>CF*</i>	<i>16</i>	<i>64 ports</i>	<i>2 (10 GbE) / 4 ports</i>	<i>1 feature</i>
<i>OSA-Express3-2P GbE</i>	<i>CF*</i>	<i>16</i>	<i>32 ports</i>	<i>2 ports</i>	<i>1 feature</i>
<i>OSA-Express2**</i>	<i>CF</i>	<i>16</i>	<i>32 ports</i>	<i>2 ports</i>	<i>1 feature</i>
<b>Crypto***</b>					
<b>Crypto Express3</b>	<b>NB</b>	8	16 PCIe adapters	2 PCIe adapters	1 feature***
<b>Crypto Express3-1P</b>	<b>NB</b>	8	8 PCIE adapters	1 PCIe adapter	1 feature***



\* Can be carried forward or ordered by MES using RPQ 8P2534 if adding PCIe I/O features is not possible

\*\* OSA-Express2 10 GbE LR is not supported as a carry forward

\*\*\* Two features initially, one thereafter

**NB = New Build**  
*CF = Carry Forward*

## z114 and z196 GA2 InfiniBand Coupling Fanouts

Description	F/C	Ports	Comments
HCA3-O 12x IB DDR 	0171	2	PSIFB coupling (150 m) <b>Improved responsiveness</b> (HCA3-O to HCA3-O)
HCA3-O LR 1x IB DDR 	0170	4	PSIFB coupling (10 km unrepeated, 100 km with DWDM) <b>Double port density. More subchannels per CHPID.</b>
HCA2-O 12x IB-DDR	0163	2	<b>Coupling (150 meters) Also available on z10 EC, z10 BC. Required for 12x connection to System z9 HCA1-O.</b>
HCA2-O LR 1x IB-DDR <b>Carry forward only</b>	0168	2	<b>Coupling (10 km unrepeated, 100 km with DWDM) Also available on z10 EC, z10 BC</b>
<p><b>Note: Coupling fanouts compete for slots with the HCA2-C and PCIe fanouts for I/O drawers and cages.</b></p>			

Note: The InfiniBand link data rates do not represent the performance of the link. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.

## z114 and z196 GA2 Parallel Sysplex Coupling Connectivity

### z9 EC and z9 BC S07

IFB 12x SDR, ISC-3

**z9 to z9 IFB is NOT supported**



HCA1

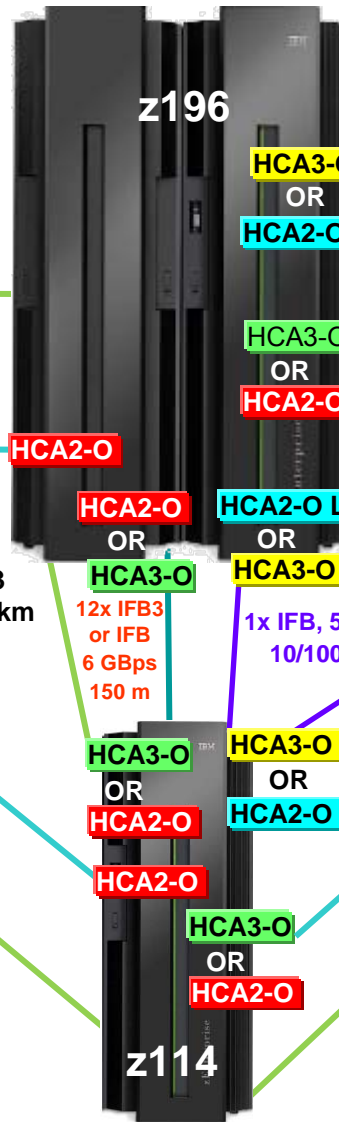
ISC-3, 2 Gbps  
10/100 km

12x IFB, 3 GBps  
Up to 150 m

ISC-3, 2Gbps, 10/100 km

12x IFB, 3 GBps, 150 m

### z196



HCA3-O LR

OR

HCA2-O LR\*

HCA3-O

OR

HCA2-O

HCA2-O

OR

HCA3-O

HCA3-O

OR

HCA2-O

HCA3-O

OR

HCA2-O

### z114

ISC-3  
10/100 km

12x IFB3  
or IFB  
6 GBps  
150 m

1x IFB, 5 Gbps  
10/100 km

HCA3-O LR

OR

HCA2-O LR\*

HCA3-O

OR

HCA2-O

1x IFB, 5 Gbps  
10/100 km

ISC-3, 2 Gbps  
10/100 km

12x IFB, 6 GBps  
150 m

1x IFB, 5 Gbps, 10/100 km

12x IFB, 6 GBps, 150 m

ISC-3, 2 Gbps, 10/100 km

### z10 EC and z10 BC

IFB 12x and 1x, ISC-3,



HCA2-O LR

HCA2-O

HCA2-O LR

HCA2-O

**Note: ICB-4 and ETR are NOT supported on z196 or z114**

\*HCA2-O LR carry forward only on z196 and z114

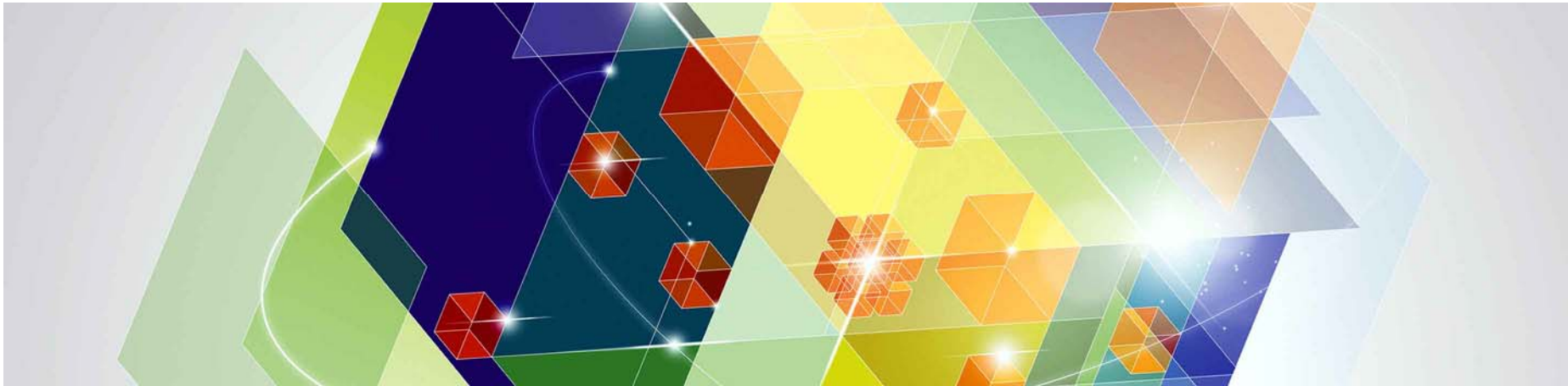
**Note:** The InfiniBand link data rates do not represent the performance of the link. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.



**z800, z900  
z890 and z990**  
*Not supported!*

# zEnterprise Physical Planning

System z – Freedom Through Design

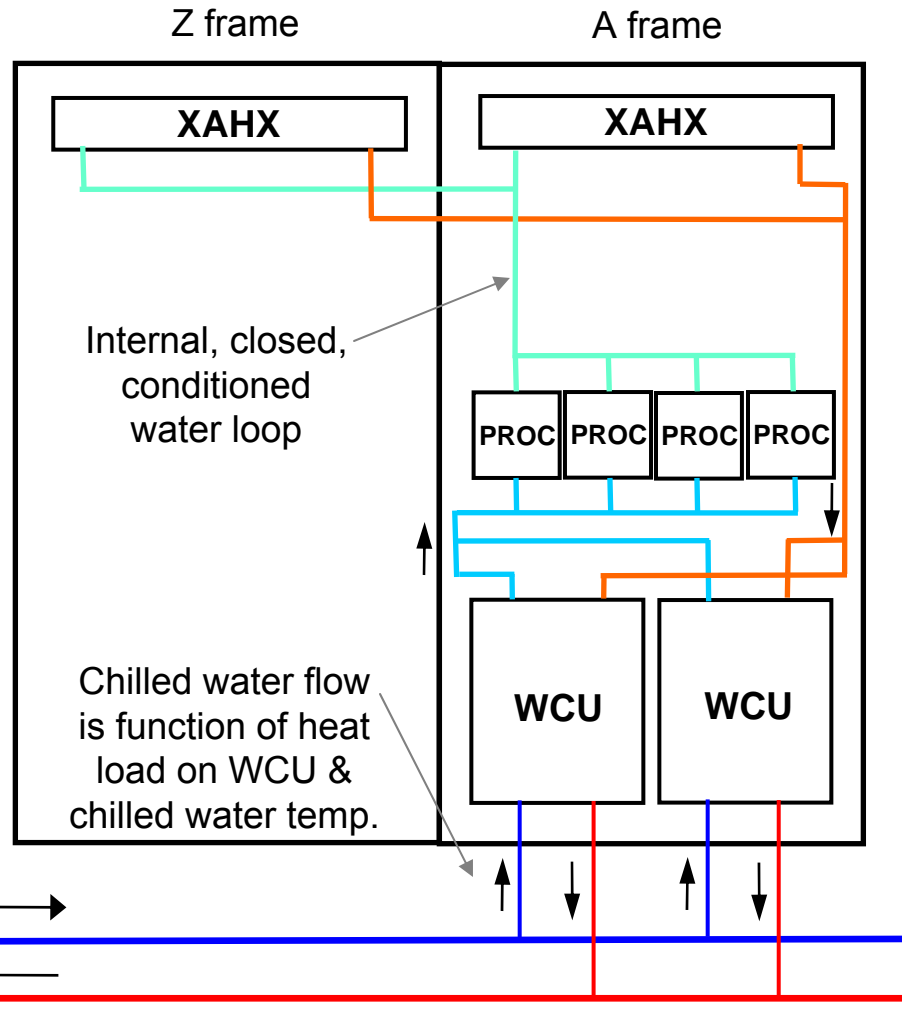


## z196 optional water cooling



Infrastructure

Not to scale, not physically representative



- A Smarter IT for a Smarter Planet™
- Each book has a water cooled cold plate for the processor MCM
- Water Cooling Unit (WCU) design is N+1 with independent chilled water connections
  - One WCU can support system without cycle steering
  - Connects to ordinary building chilled water (like AC units and unlike water cooled rear doors)
- Rear Door Exhaust Air Heat Exchanger (XAHX)
  - Removes heat from exhaust air at back of both frames
  - Provides an air cooling back-up mode for robustness
- Designed to reduce the heat load exhausted to air by 60-65%
  - ~10 kW system heat load to air maximum (5 kW per frame)
  - ~2 kW Input energy savings for a maximum power system
  - ~2.5 kW additional power savings to cool the reduced air heat load

*The water cooling option must be ordered with a new build or machine type upgrade. It is not available as a z196 MES change after installation.*

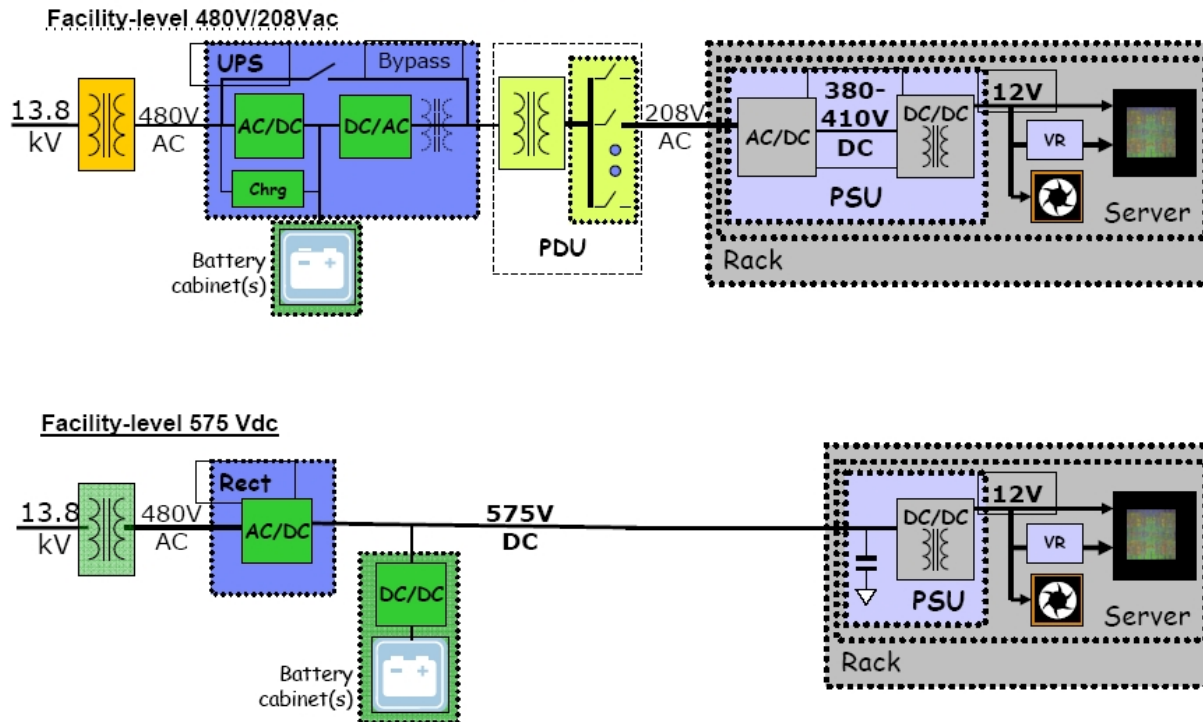
## z196 optional high voltage DC power

- A Smarter IT System for a Smarter Planet
- Using high voltage DC power can save, on average, 1 to 3% of power by eliminating DC to AC and AC to DC conversion losses



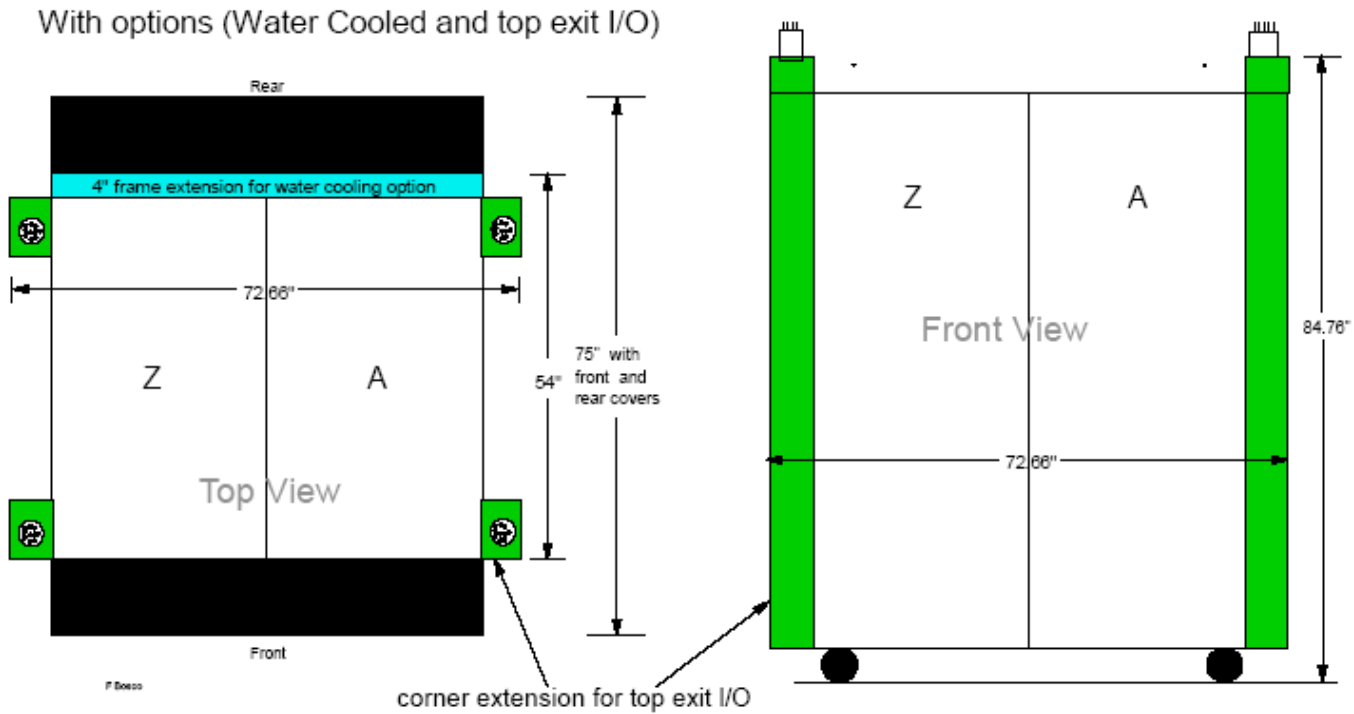
Infrastructure

### AC vs DC Distribution



## System z196 with optional water cooling and Overhead I/O Dimension changes compared to the z10 EC

- Depth: Water Cooled option adds 4 inches to the rear (with reference to floor cutouts)
- Width: Overhead I/O Option adds 11 -12 inches side to side  
5.5 – 6 inches to the outside edge of the A and Z frames (with reference to floor cutouts)
- Height: Overhead I/O Option adds 5.5 – 6 inches (Reduced height shipping to 71 inches available)
- Weight: Overhead I/O Option adds ~ 200 pounds, Water Cooled Option adds ~ 100 pounds
- z196 must be installed on a raised floor



**Note: All dimensions are approximate**



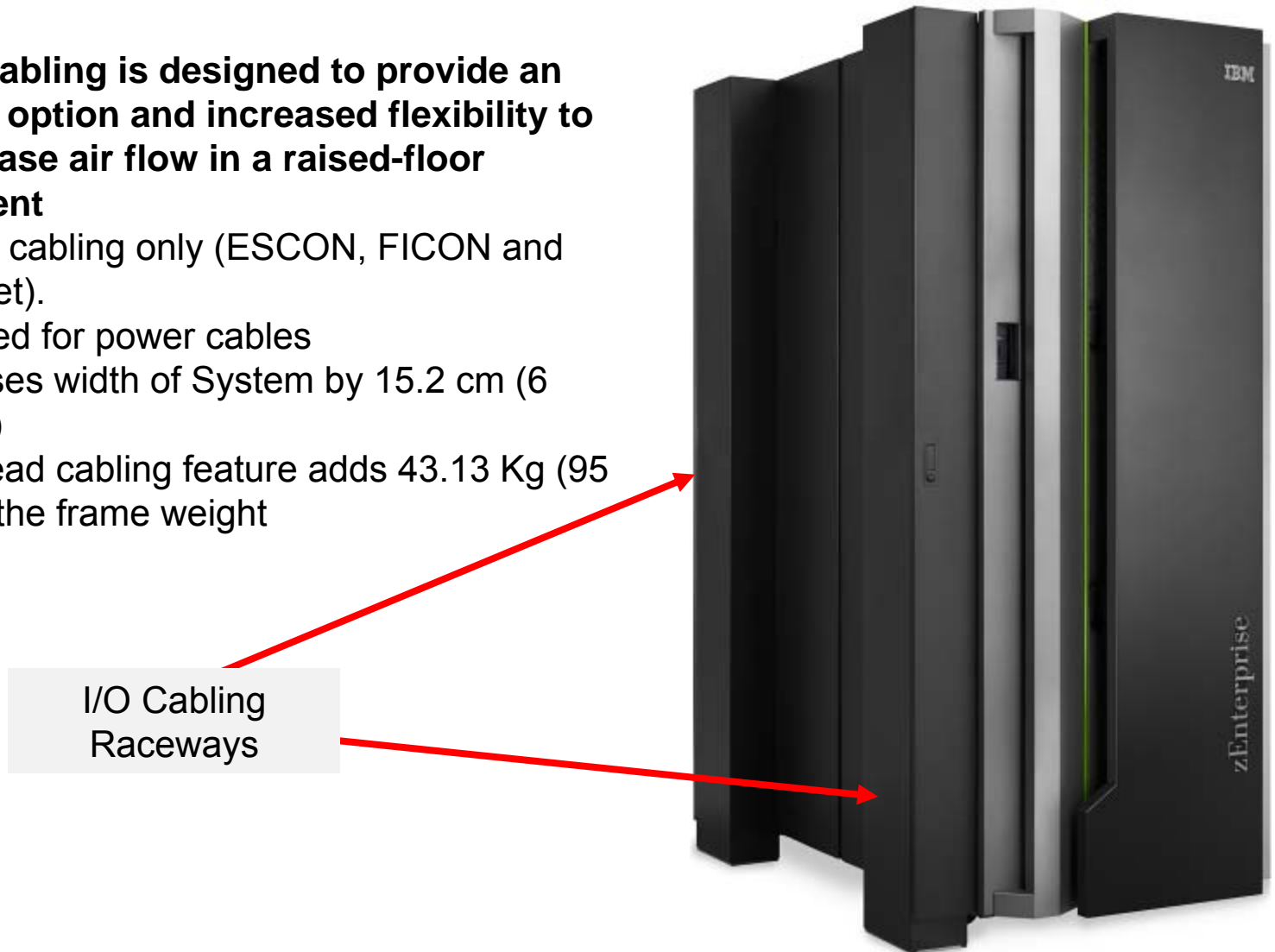
## Built to support future data center design, modernization and efficiencies

- **More performance and capacity within the same energy envelope as the z10 BC**
- **Supports raised floor and non-raised floor configurations**
- **Improved installation flexibility with overhead cabling option**
- **Reduced footprint depth by 9" (22.8 cm) compared to z10 BC**
- **Optional high-voltage DC power input**



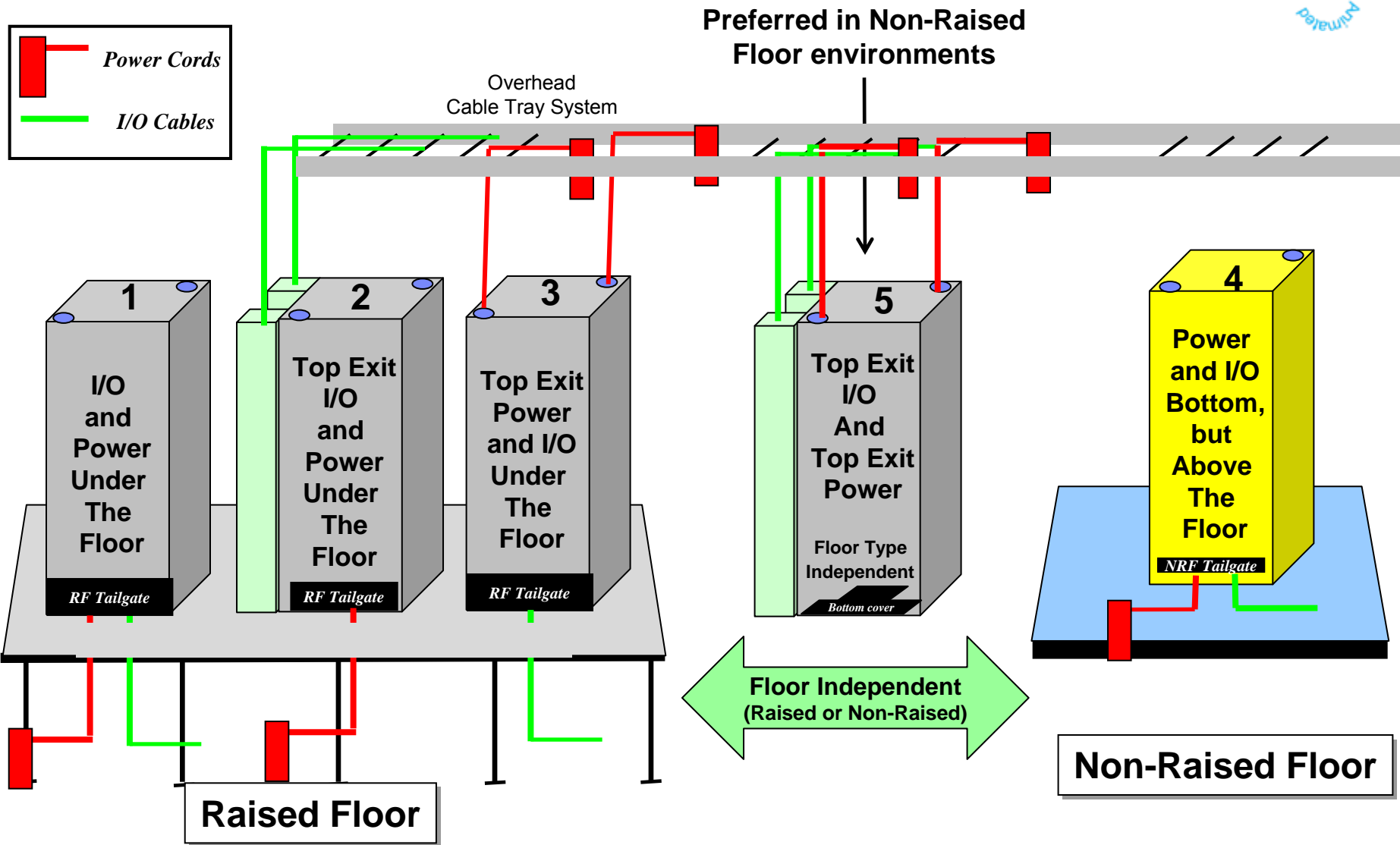
## z114 Overhead I/O Cabling Option

- **Top Exit cabling is designed to provide an additional option and increased flexibility to help increase air flow in a raised-floor environment**
  - For I/O cabling only (ESCON, FICON and Ethernet).
  - Not used for power cables
  - Increases width of System by 15.2 cm (6 inches)
  - Overhead cabling feature adds 43.13 Kg (95 lbs) to the frame weight



## z114 Floor and Cabling Configurations options

Animated  
Animated



## Removal of HMC Dial Modem Support (October 12, 2011 Statement of Direction<sup>1</sup>)



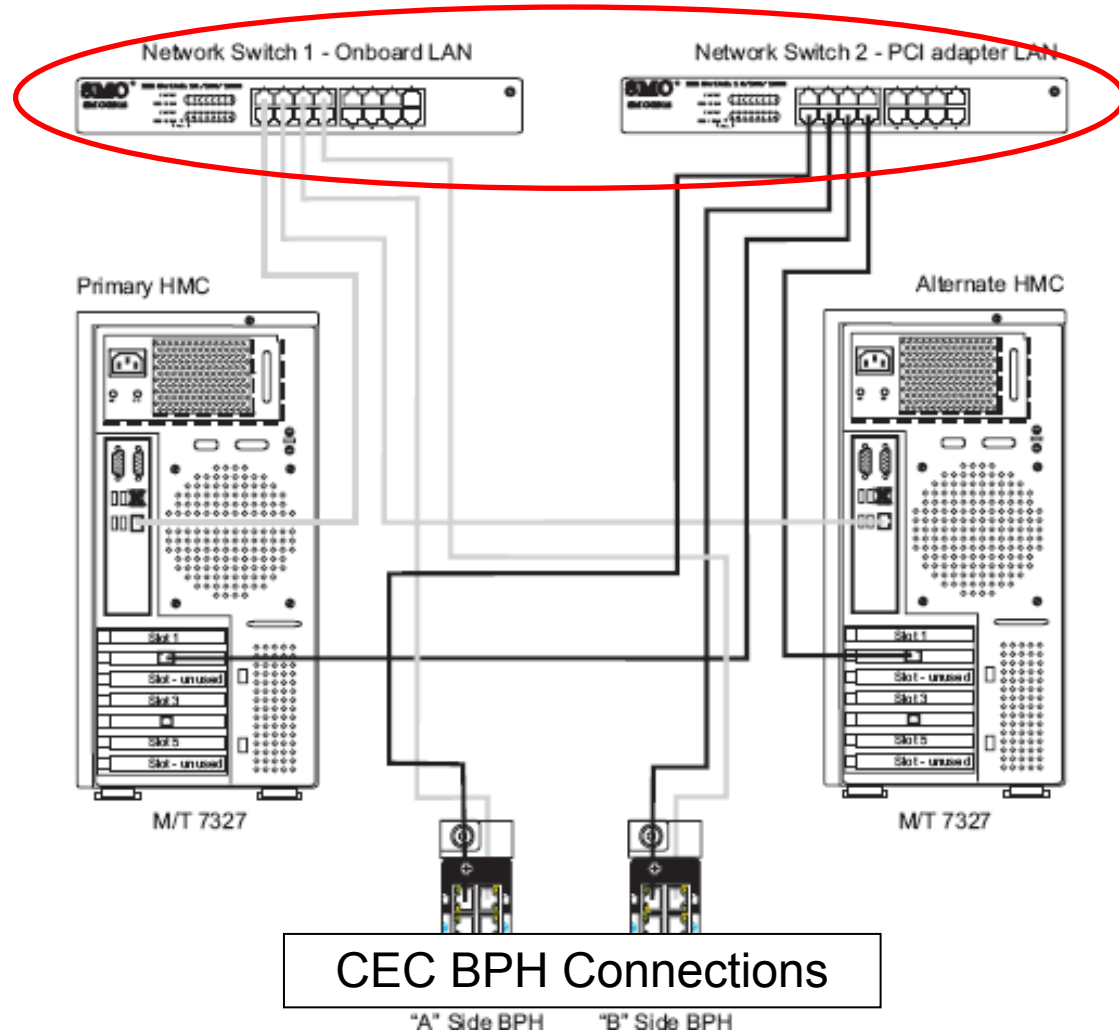
- **Beginning with the next System z server after the IBM zEnterprise 196 and 114, the new Hardware Management Console (HMC) LIC is intended no longer to provide modem support.** As a result, it will no longer be possible to use dial access to the Remote Support Facility (RSF) or to access an External Time Source (ETS) for Server Time Protocol (STP). Only broadband connections will be allowed. The new HMC LIC is planned to support Network Time Protocol (NTP) authentication support to provide enhanced security when an NTP server is accessed to get accurate time for the STP Coordinated Timing Network (CTN).
- **Enterprises using modems for RSF or STP should plan to migrating to broadband connections.** The currently available NTP server option for ETS, as well as internet time services available using broadband connections, can be used to provide the same degree of accuracy as dial-up time services.  
Reference: [Integrating the Hardware Management Console's Broadband Remote Support Facility into your Enterprise, SC28-6880](#)
- **Note:** When implemented, the above changes are intended to apply to new HMC orders for z196 and z114, as well as upgrades of older HMCs to this new version of HMC LIC.

<sup>1</sup> All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of General Direction is at the relying party's sole risk and will not create liability or obligation for IBM.

## End of Marketing for System z Server Ethernet Switch Features (October 12, 2011 Statement of Direction<sup>1</sup>)



- IBM intends that the zEnterprise 196 and zEnterprise 114 will be the last servers to offer ordering of the external Ethernet switch.**
- As a result, it will no longer be possible to order as server features on future System z servers the Ethernet switches required to by HMCs. Customers should plan to use existing supported switches or to acquire additional switches separately to implement the required HMC LAN connectivity.
- Note:** Ethernet switches are offered today as FC #0070 on zEnterprise servers.



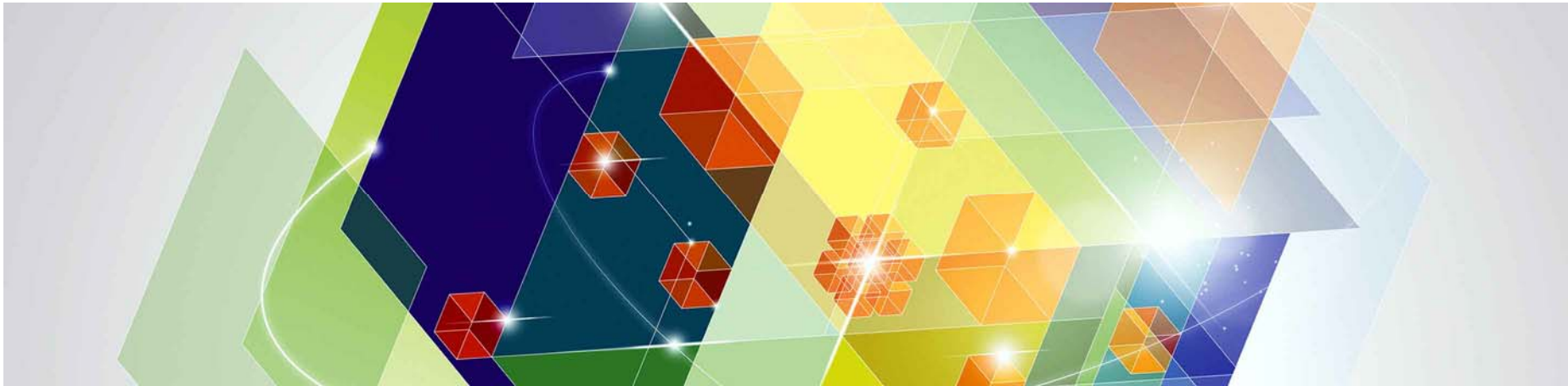
<sup>1</sup> All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of General Direction is at the relying party's sole risk and will not create liability or obligation for IBM.

**Thank you!**  
**[ibm.com/systems/z](http://ibm.com/systems/z)**



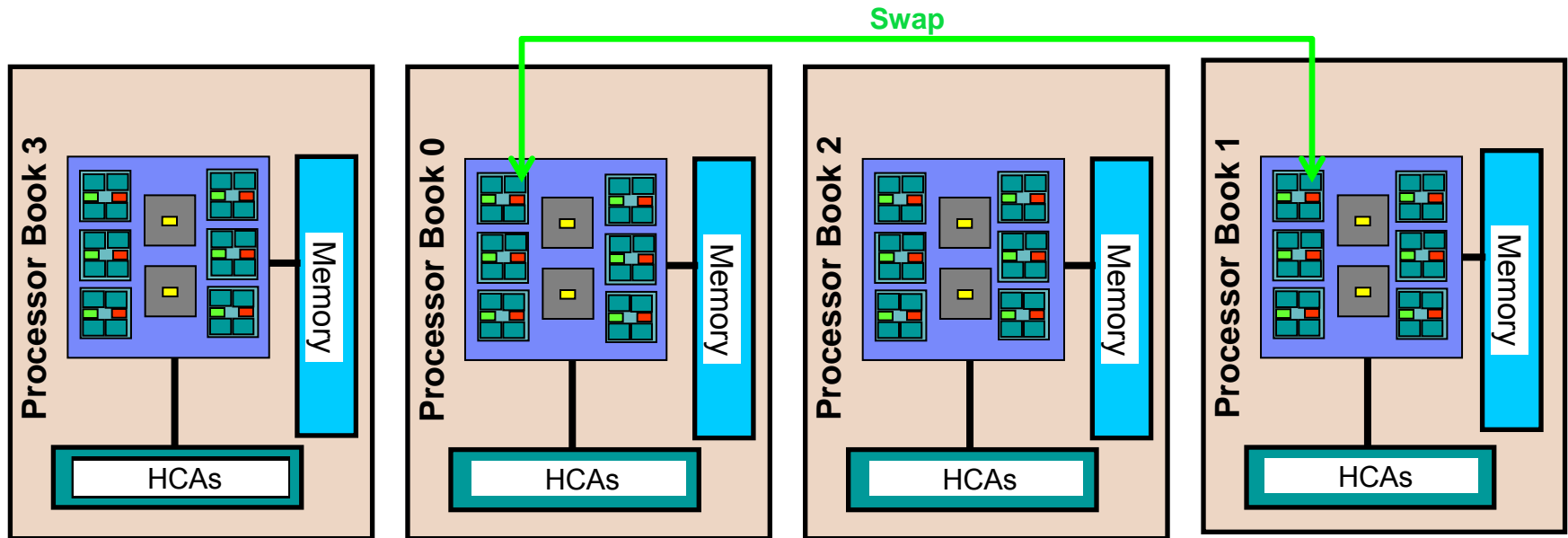
## Backup Charts

### System z – Freedom Through Design



## z196 LPAR Dynamic PU Reassignment

- PR/SM dynamic relocation of running processors to different processor cores
- Designed to optimize physical processor location for the current LPAR logical processor configuration
- Swap an active PU with a different active PU in a different book
  - Designed Benefit: Better L3 and L4 cache reuse
  - CP, zAAP, and zIIP are supported
  - Triggers: Partition activation/deactivation, machine upgrades/downgrades, logical processors on/off
- Designed to provide the most benefit for:
  - Multiple book machines
  - Dedicated partitions and wide partitions with HiperDispatch active





## z196 Plan Ahead Memory

- **Provides the capability for concurrent memory upgrades without exploitation of Enhanced Book Availability, Licensed Internal Code upgrades**
  - Memory cards are pre-installed to support target Plan Ahead capacity
  - Available on all System z196 models
  - Can be ordered with standard memory on any z196 model  
(*Standard plus Plan Ahead will NOT be Flexible in most cases.*)
  - Can be ordered with Flexible memory on a multiple book z196 model
  
- **Pre-planned memory features are chargeable**
  - Charge for memory hardware needed to enable the selected plan ahead target.
  - FC #1996 – One feature for each 16 GB (20 GB RAIM) of additional hardware needed
  
- **Pre-planned memory activation is chargeable**
  - Subsequent memory upgrade orders will use Plan Ahead Memory first
  - Charged when Plan Ahead Memory is enabled by concurrent LIC upgrade
  - Add FC #1901, Delete FC #1996 – For each 16 GB of memory activated for use
  
- **Note: Plan Ahead Memory is NOT temporary, On Demand memory**  
*Temporary memory is not offered because Memory LIC downgrade is disruptive.*

## Current ESCON Statement of Direction\* July 12, 2011 Announcements

- **The IBM zEnterprise 196 and the IBM zEnterprise 114 will be the last System z servers to support ESCON channels:** IBM plans not to offer ESCON channels as an orderable feature on future System z servers. In addition, ESCON channels **cannot be carried forward** on an upgrade to such follow-on servers. This plan applies to channel path identifier (CHPID) types CNC, CTC, CVC, and CBY and to featured 2323 and 2324. System z customers should continue migrating from ESCON to FICON. Alternate solutions are available for connectivity to ESCON devices. IBM Global Technology Services offers an ESCON to FICON Migration solution, Offering ID #6948-97D, to help simplify and manage an all FICON environment with continued connectivity to ESCON devices if required.
- Notes:
  - For z196, this new Statement of Direction restates the SOD in Announcement letter 111-112 of February 15, 2011. It also confirms the SOD in Announcement letter 109-230 of April 28, 2009 that “ESCON Channels will be phased out.”

\*All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these statements of general direction is at the relying party's sole risk and will not create liability or obligation for IBM.

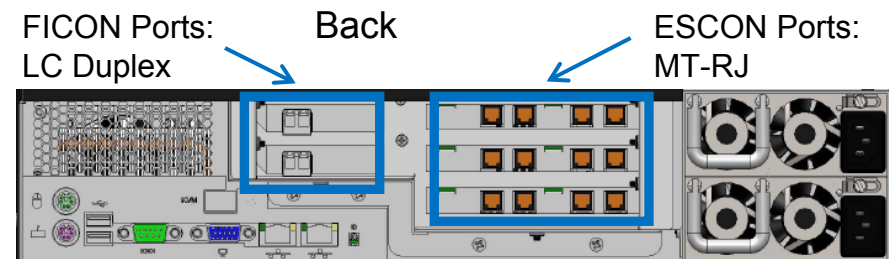
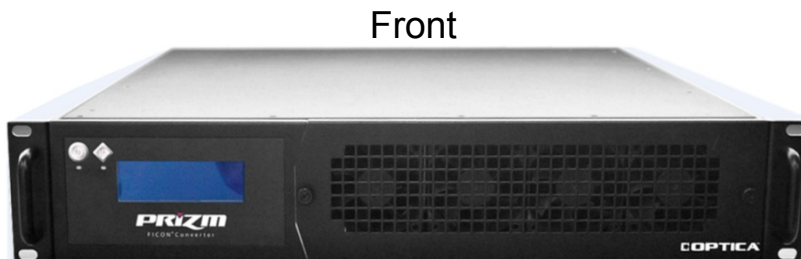
## Optica PRIZM FICON Converter

<http://www.opticatech.com/>

Supports the elimination of ESCON channels on the host while maintaining ESCON and Bus/Tag-based devices and applications

### What is PRIZM?

- A purpose-built appliance designed exclusively for IBM System z; enables ESCON devices to be connected to FICON channels or fabrics
- Allows ESCON devices to connect to FICON channels and FICON fabrics/networks
  - Prizm also supports attachment of parallel (bus/tag) devices to FICON channels via ESBT module
- Converts 1 or 2 FICON channels (CHPID type FC) into 4, 8 or 12 ESCON channels
  - Replace aging ESCON Directors with PRIZM (maintenance savings)
  - Achieve streamlined infrastructure and reduced Total Cost of Ownership
- Qualified by the IBM Vendor Solutions Lab in POK for all ESCON devices; qualified for connectivity to Brocade and Cisco FICON switching solutions
  - Refer to: <http://www-03.ibm.com/systems/z/hardware/connectivity/index.html>
    - Products -- > FICON / FCP Connectivity -- > Other supported devices
- PRIZM is available via IBM Global Technology Services: ESCON to FICON Migration offering (#6948-97D)



## Current Power Sequence Controller Statement of Direction\*

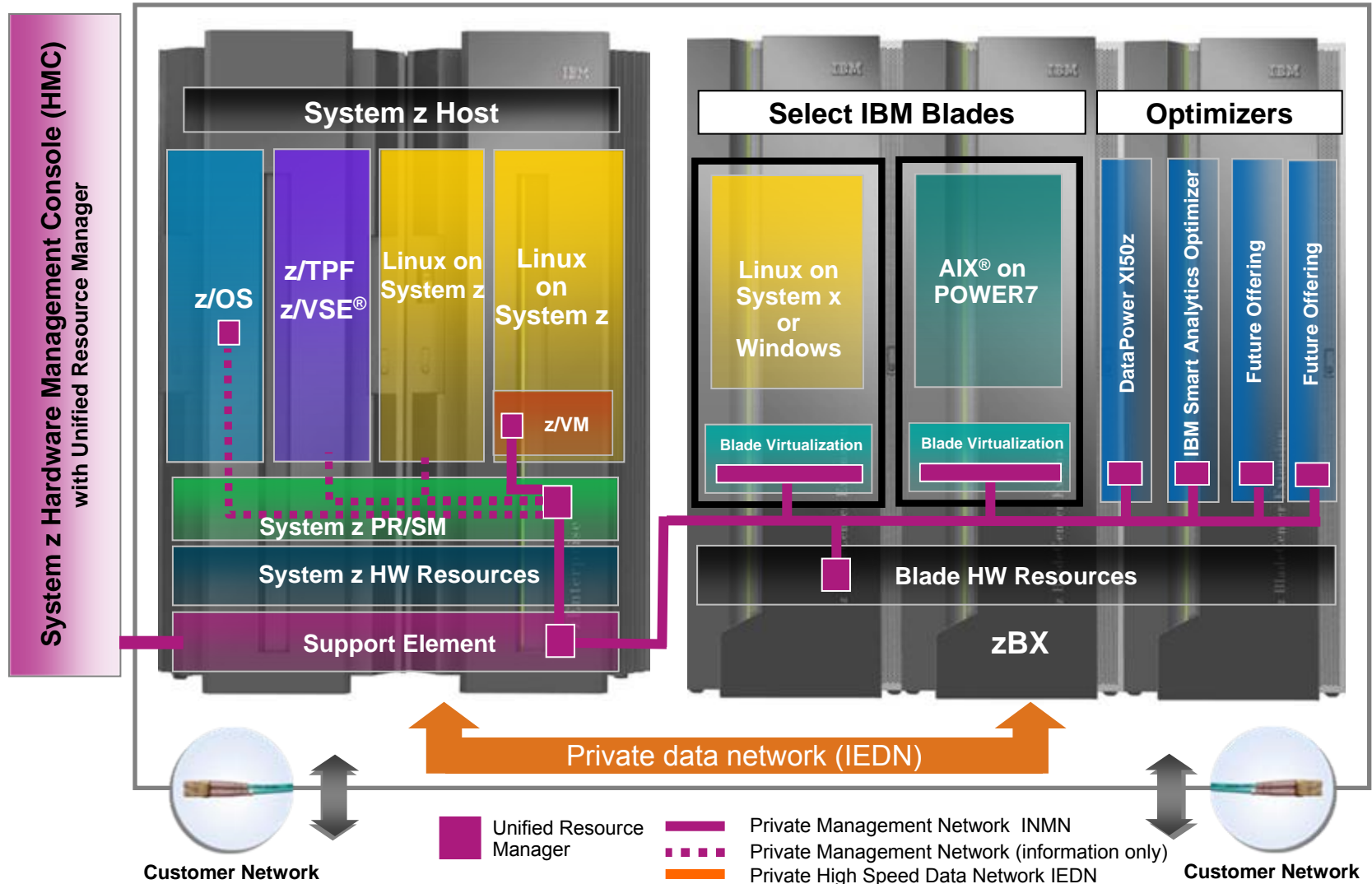
### July 12 , 2011 Announcements

- **The IBM zEnterprise 196 and the zEnterprise z114 are the last System z servers to support the Power Sequence Controller (PSC) feature.** IBM intends to not offer support for the PSC (feature #6501) on future System z servers after the z196 (2817) and z114 (2818). PSC features cannot be ordered and cannot be carried forward on an upgrade to such a follow-on server.
  
- **Notes:**
  - This is a revision to the PSC statement of general direction published October 20, 2009, IBM System z10 - Delivering Security-Rich Offerings to Protect Your Data, Hardware Announcement 109-678.
  
  - The PSC optional feature provides the ability to power control units with the required hardware interface on and off from the System z server.

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## Putting zEnterprise System to the Task

*Use the smarter solution to improve your application design*



**Last Chart!**  
[ibm.com/systems/z](http://ibm.com/systems/z)

